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Simulated Channel Length Variation Effects on Regulated Cascode Input Stage-Based Transimpedance Amplifier for Fiber Optics Applications

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***Abstract*— A proposed transimpedance amplifier with channel length variation is simulated. The amplifier consists of a regulated cascode input stage followed by a common gate-common source configuration. A channel length series (45 nm, 90 nm and 130 nm) in CMOS technology was introduced within the proposed amplifier in order to achieve comparative performance analysis. There are two key findings from this study. On one hand, it was found that the trade off in gain versus bandwidth and input referred noise current still applies when channel length is moved upward from 45 nm up to 130 nm. A series of transimpedance amplifier gains (42.16 dBΩ, 44.34 dBΩ and 46.25 dBΩ) that correspond to (1.80 GHz, 1.33 GHz and 1.06 GHz) of f_{-3dB} bandwidths is reported corresponding to the above channel length series respectively with an input referred noise current spectral density series (16.35 $pA/\sqrt{Hz}$, 12.17 $pA/\sqrt{Hz}$ and 10.60 $pA/\sqrt{Hz}$) of reduction. On the other hand, a reduction in power consumption occurred as channel length is moved upward for the same proposed topology. A total power consumption series (0.611 mW, 0.287 mW and 0.173 mW) was reported that corresponds to the above channel length series.**

***Index Terms*— Feedforward; Front-End Preamplifier; RGC; Transimpedance Amplifier.**

I. Introduction

A growing demand for efficient fiber optical communication links imposed certain criteria on front-end optical preamplifiers. A 45 nm silicon-on-insulator "S.O.I.," CMOS process was demonstrated in a form of 40 Gb/s optical transceiver that consists of a transimpedance amplifier (TIA) where a feedback resistor is connected between the gate and drain of NMOS and PMOS transistors [1]. A two phases TIA namely a regulated cascode RGC and an inverted cascode output stage was demonstrated in 45 nm CMOS process [2]. A TIA using 45 nm and 180 nm inductorless CMOS process was achieved in which a single-ended current-mode TIA in a form of N similar TIAs in parallel configuration was reported [3]. A modified RGC TIA followed by a closed loop gain stage with an added level shifter circuit to the booster of a conventional RGC circuit was proposed in 90 nm CMOS process [4]. A TIA with three cascaded stages in a form of common source amplifiers utilizing capacitive degeneration and inductive peaking in 90 nm CMOS process was introduced [5]. A 90 nm CMOS TIA with high-linearity was designed with regulated cascode (RGC) input stage with active feedback replacing feedback resistor to reduce chip size [6]. A 5 Gbps TIA in 90 nm CMOS process was introduced that employs an active RGC structure at the input stage that led to low input resistance which was followed by a level shifter and a common source structure to achieve high transimpedance at low supply voltage [7]. A 64-Gbaud TIA in 130 nm SiGe process was implemented. The topology involved a π–network broadband technique and shunt-shunt RC feedback to achieve high gain and a wide bandwidth [8]. A double cascode TIA with inductive peaking and shunt-shunt negative feedback was realized in 130 nm RF CMOS process for 10 Gbps optoelectronic receivers [9]. A 2.5 Gbit/s TIA was realized in 130 nm CMOS technology that involved using a common source (CS) amplifier with active inductive peaking [10]. Past TIA models were realized in 0.18 μm CMOS process that involved shunt-shunt feedback and differential topologies for the sake of variable gain and moderately high bandwidth at the expense of power consumption [11].

The main objective of this work is to find out that the trade-off in gain versus bandwidth and input referred noise current still applies when channel length is moved upwards from 45 nm towards 130 nm. In addition, to show a considerable reduction in power consumption and input referred noise current using the proposed topology especially when channel length is increased.

II. Proposed Topology

A. Regulated Cascode Input Stage

In comparison with common-gate (CG) topology, the RGC TIA structure as in Fig. 1 adds another transistor M_2 as a booster amplifier that can lead to a rise in the transconductance of transistor M_1 by a factor of $(1 + g_{m2}R_B)$ in which the input resistance can be represented as [4]:

$$R_{in} = \frac{r_{O3}}{1+g_{m1}r_{O3}(1+g_{m2}R_B)} \quad (1)$$

where r_{O3} is the output resistance of transistor M_3

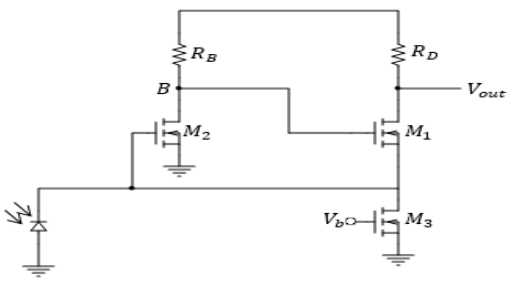

Fig. 1. Classic RGC TIA Topology [4].

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Based on the above concept, the proposed topology takes into account that typical CG structure may not totally isolates the influence of input parasitic capacitance, however, the RGC input node $in1$ relaxes the effect of large input parasitic capacitance on bandwidth to a considerable extent as in Fig. 2. In addition, it should be able to mitigate certain constraints on power consumption with improvement in noise performance compared with CG topology. Since node $in1$ sits at virtual ground, the effective transiconductance is enhanced to some extent. The $M_1 - r_{O8}$ path (drain current path between r_{O1} to r_{O8}) works as a local feedback that is to lower input impedance in an identical scale to that of its own voltage gain. However, within the system transfer function, this local feedback produces a zero pole. In the frequency response, a certain peaking is expected that can be specified at the frequency $1/[2\pi r_{O8}(C_{gs2} + C_{db1})]$. This peaking can be scaled down when r_{O8} or the gate width of transistor $M_2$is reduced. The advantage of the local feedback is that it applies high impedance at the drain node of transistor M_2, hence moving the RGC dominant pole to a higher frequency *i.e.* widening the bandwidth. The voltage gain in the CS configuration of transistor M_2 equals to $g_{m2}.(r_{O9} \| r_{O2} \| r_{O4})$. The pass transistor M_4 raises dc voltage level of the subsequent CG-CS stage input node $in2$,.thus provides enough voltage headroom for transistorM_6 to conduct drain current suffeciently, therefore enabling voltage gain at node B that is transformed onto node O_2.

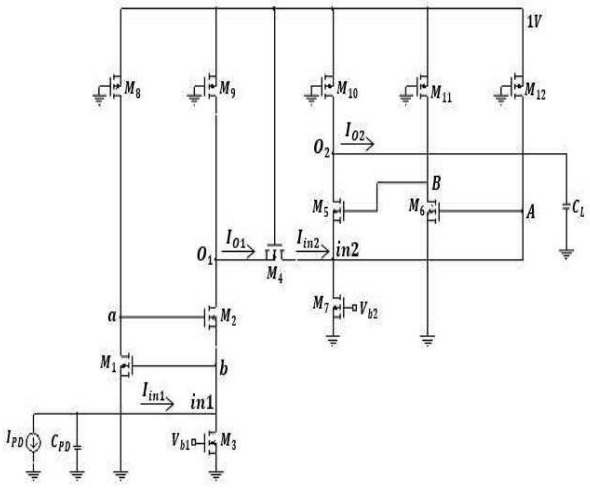


Fig. 2. Proposed TIA Topology.

The small signal equivalent circuit model of the RGC TIA input stage is manifested in Fig. 3.The total capacitance to ground from node a is represented as C_a in which $C_a = C_{gb2} + C_{db1} + C_{db8}$. At input node $in1$, the total parasitic capacitance to ground is C_b in which $C_b = C_{PD} + C_{gb1} + C_{sb2}$ through which the photodiode capacitance C_{PD} dominates where C_{gb1} is the gate-to-bulk capacitance for transistor M_1, while is the soure-to-bulk capacitance of transistor M_2. The gate-to-source capacitance of transistor M_2 and gate-to-drain capacitance of transistor M_1 summation are combined as $C_{ab} = C_{gs2} + C_{gd1}$. The output node O_1 capacitance is buffered from the the subsequent CG-CS stage by the pass transistor M_4. The drain-to-bulk parasitic capacitance of M_4 is in parallel with CG-CS input stage capacitance.

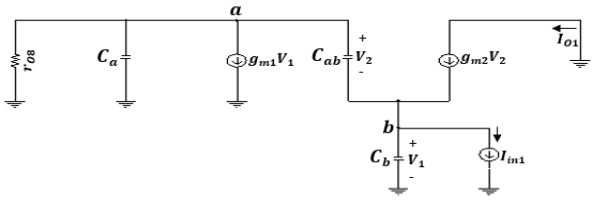


Fig. 3. RGC small signal equivalent circuit model.

B. *Overall TIA Gain*

Based on Kirchhoff current law "K.C.L.," the following representations are established for the RGC input stage according to the small signal model of Fig. 3:

$$(V_1 + V_2) \cdot \frac{1}{r_{O8}} + (V_1 + V_2)sC_a + g_{m1}V_1 + V_2sC_{ab} = 0 \quad (2a)$$

$$V_2sC_{ab} + g_{m2}V_2 = V_1sC_b + I_{in1} \quad (2b)$$

$$I_{O1} = g_{m2}V_2 \quad (2c)$$

The deduced current gain Equation becomes:

$$\frac{I_{O1}}{I_{in1}} = \frac{N_1 + sN_2}{D_1s^2 + D_2s + D_3} \quad (3)$$

Where, $N_1 = g_{m2}(1 + g_{m1}r_{O8})$, and $N_2 = C_a r_{O8} g_{m2}$, while $D_1 = r_{O8}(C_{ab}C_a + C_{ab}C_b + C_aC_b)$, $D_2 = C_{ab} + r_{O8}(C_{ab}g_{m1} + C_a g_{m2}) + C_b$ and $D_3 = N_1$. Transconductance parameter g_{mx} are defined as per each transistor number and so as the output resistance r_{Ox}.

The input impedance of the RGC TIA input stage structure is:

$$Z_{in1} = \frac{E_1 + sE_2}{F_1s^2 + F_2s + F_3} \quad (4)$$

Where, $E_1 = 1/r_{O8}$ and $E_2 = C_a + C_{ab}$, while $F_1 = C_aC_{ab}$, $F_2 = C_{ab}(1 + (1/r_{O8}) + g_{m1}) + C_a g_{m2}$ and $F_3 = g_{m2}\big((1/r_{O8}) + g_{m1}\big)$. A change of phase in terms of input impedance in a form of changing phase from input signal current I_{in1} (going to node $in1$) to input signal voltage V_{in1} (at node $in1$) can occur, Since the dc input resistance $R_{in1} = E_1/F_3$, the f_{-3dB} bandwidth is therefore considered to be:

$$f_{-3dB} = \frac{1}{2\pi R_{in1} C_{in1,tot}} \quad (5)$$

Where the total input parasitic capacitance $C_{in1,tot} = C_b$ in which the decrease in input resistance while minimizing $C_{in1,tot} = C_b$ results in wider bandwidth.

The small signal equivalent circuit model of the CG-CS subsequent stage is shown as in Fig. 4. The input node $in2$ accommodates voltage swing V_{in2} that is in parallel with total input parasitic capacitances $C_{in2,tot}$ and the positive side of C_{gs5}. Evidently, from node A stand point, a voltage dropV_{gs6} is across drain-to-source resistor r_{ds12} of transistor M_{12}. Parasitic capacitance sits at near virtual ground since there is not much of a voltage difference between node $in2$ and A. A fractional part of the drain current $g_{m6}V_A$ feeds into node B that counter balance the charge in the negative side of C_{gs5} as the voltage difference between nodes B and $in2$ is V_{gs5} and that is the gate-to-source voltage swing for transistor M_5.

Consequently, the output node O_2 is fed by the drain current $g_{m5}(V_B - V_{in2})$.

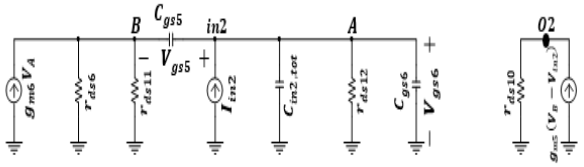


Fig. 4. A small signal equivalent circuit for the CG-CS stage.

Following on "K.C.L.," equations and based on small signal model for the CG-CS subsequent stage, parasitic capacitances $C_{g5}, C_{d5}, C_{d6}$and C_{d12} are also included, while $sC_{gd5} \ll 1 <<$, $sC_{g6} \ll$ and $sC_{gd6} \ll 1$.

$$I_{in2} = V_{in2}(g_{m5} + g_{mb5} + g_{ds5} + g_{ds7} + sC_{in2,tot}) - V_B(g_{m5} + sC_{gs5}) - V_{O2}(g_{ds5} + sC_{ds5}) \quad (6a)$$

$$0 = V_A\left(g_{ds12} + s\left(C_{d12} + C_{gb6}\right)\right) - V_B sC_{gd6} - V_{in2} sC_{gb6} \quad (6b)$$

$$0 = V_B\left(g_{ds11} + g_{ds6} + s\left(C_{db6} + C_{gb5} + C_{d11}\right)\right) - V_A(g_{m6} - sC_{gd6}) - V_{O2} sC_{gd6} \quad (6c)$$

$$0 = V_{O2}(g_{ds10} + g_{ds5} + s(C_{db5} + C_{db10})) + V_B(g_{m5} - sC_{gd5}) - V_{in2}(g_{m5} + g_{mb5} + g_{ds5} + sC_{gd5}) \quad (6d)$$

Bulk Transconductance parameter g_{mbx} are defined as per each transistor number, drain-to-source conductance as g_{dsx}, gate-to-source parasitic capacitances as C_{gsx}, drain-to-bulk parasitic capacitances as C_{dbx} and C_{gbx} is the gate-to-bulk parasitic capacitance.

A transfer of impedance from node $in2$ to node A with no actual voltage gain is shown in "(7)," however, the following formula is envisaged based on "(6b)," for the sake of representation:

$$A_{in2A} = \frac{V_A}{V_{in2}} = \frac{sC_{g6}}{g_{ds12} + s(C_{db12} + C_{gb6})} \quad (7)$$

The voltage gain from node A to node B is given as:

$$A_{AB} = \frac{V_B}{V_A} = \frac{g_{m6}}{g_{ds11} + g_{ds6} + s(C_{db6} + C_{gb5} + C_{d11})} \quad (8)$$

The voltage gain of the CG-CS stage is represented by:

$$A_{v2} = \frac{V_{O2}}{V_{in2}} = \frac{g_{m5}(1 + |A_{in2A}A_{AB}| + g_{mb5} + g_{ds5}}{g_{ds10} + g_{ds5} + s(C_{db5} + C_{db10})} \quad (9)$$

The input impedance of the CG-CS stage is manifested as follows:

$$Z_{in2} = \frac{1}{P + sC_{eq2}} \quad (10)$$

Whereas fractional P is given as:

$$P = g_{m5}(1 + |A_{in2A}A_{AB}|) + g_{mb5} + g_{ds5} + g_{ds7} - A_{v2}g_{ds5} \quad (11)$$

As the equivalent input capacitance for the CG-CS stage is $C_{eq2} = C_{in2,tot} + |A_{in2A}A_{AB}|C_{gs5}$, while the CG-CS TIA gain is:

$$Z_{TIA2} = \frac{V_{O2}}{I_{in2}} = Z_{in2}A_{v2} \quad (12)$$

The overall TIA gain for the proposed TIA topology becomes:

$$Z_{TIA} = \frac{I_{O1}}{I_{in1}} \times \frac{V_{O2}}{I_{in2}} \quad (13)$$

Given that $I_{O1} = I_{in2}$, the above equation is a current gain of the RGC input stage multiplied by the TIA gain of the CG-CS stage.

C. Noise Analysis

The noise small signal equivalent circuit model for the RGC input stage is schematically shown in Fig. 5.

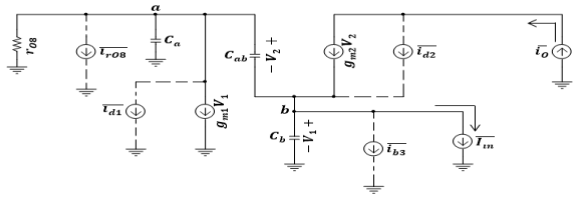


Fig. 5. The ac equivalent circuit of the noise model of the RGC input stage.

The output noise current $\overline{i_{O1}}$ (of transistor M_1) is due to the thermal noise of the current source $\overline{i_{b3}}$ in which transistor M_3 works as a current source instead of being mere a mosfet working as a degenerated resistor as in previous literature [4]. It is directly obtained from the current gain of "(3)," that:

$$\overline{i_{O1}} = \frac{[N_1 + sN_2]\cdot\overline{i_{b3}}}{D_1s^2 + D_2s + D_3} \quad (14)$$

Whereas the output noise current $\overline{i_{O2}}$ is due to the thermal noise contribution of transistor M_2 specifically $\overline{i_{d2}}$ which is deduced based on the following "K.C.L.," equations and according to the small signal noise model of Fig. 5 by which "(2a)," is included in addition to the following Equations:

$$V_2(sC_{ab} + g_{m2}) + \overline{i_{d2}} = V_1 sC_b \quad (15a)$$

$$\overline{i_{O2}} = g_{m2}V_2 + \overline{i_{d2}} \quad (15b)$$

For which,

$$\overline{i_{O2}} = \frac{D(s)\cdot\overline{i_{d2}}}{N(s)} \quad (16)$$

Whereas:

$$D(s) = \left[\left(\left(\frac{1}{r_{O8}}\right) + sC_a g_{m1}\right)sC_{ab} + \left(\left(\frac{1}{r_{O8}}\right) + s(C_a + C_{ab})\right)sC_b\right]$$

$$N(s) = (sC_{ab} + g_{m2})\left(\left(\frac{1}{r_{O8}}\right) + sC_a + g_{m1}\right) + \left(\left(\frac{1}{r_{O8}}\right) + s(C_a + C_{ab})\right)sC_b$$

Working out $\overline{i_{O3}}$, that is due to the thermal noise contribution of transistors M_1 and M_8 drain terminals, where $\overline{i_D} = \overline{i_{d1}} + \overline{i_{d,M8}}$, hence:

$$\overline{i_{O3}} = \frac{-sC_b g_{m2}\cdot\overline{i_D}}{N(s)} \quad (17)$$

The total equivalent output noise is:

$$\overline{i^2_{O,tot}} = \overline{i^2_{O1}} + \overline{i^2_{O2}} + \overline{i^2_{O3}} \quad (18)$$

When referring the total equivalent output noise back to the input of the small signal model of Fig. 5 and based on the Van der Zeil thermal noise model [12], then:

$$\overline{i^2_{O,tot}} = \left|\frac{N_1 + sN_2}{D_1s^2 + D_2s + D_3}\right|^2 \cdot \overline{i_{in}{}^2} \quad (19)$$

The input referred noise current spectral density for the proposed TIA topology is:

$$\overline{i^2_{in}} = \overline{i^2_{d,M3}} + \left|\frac{D_1s^2 + D_2s + D_3}{N_1 + sN_2}\right|^2 \cdot \overline{i_{d2}{}^2} + \left|\frac{-sC_b g_{m2}}{N(s)}\right|^2 \cdot \overline{i_D{}^2} \quad (20)$$

For which:

$$\overline{i_{d,M3}} = \gamma 4kT g_{m3}. \quad (21)$$

As γ is the channel thermal noise coefficient.

III. RESULTS

The TIA gain in dBΩ of the proposed topology is reported in Fig. 6. For 45 nm scale, a 42.16 dBΩ is shown at a bandwidth of 1.80 GHz. The 90 nm scale simulation showed a 44.34 dBΩ at 1.33 GHz, while the 130 nm scale showed a 46.25 dBΩ at 1.06 GHz.

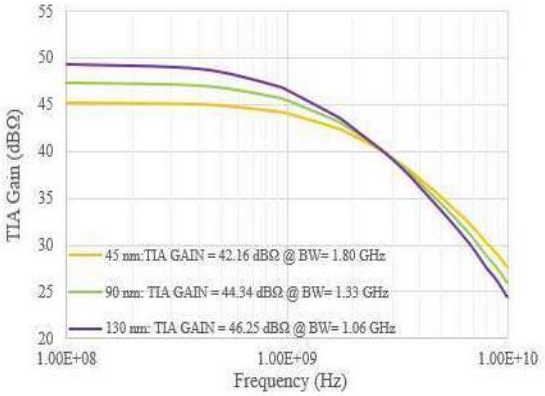


Fig. 6. TIA Gain in dBΩ for the proposed circuit.

In Fig. 7, the TIA gain in Ω is reported. For 45 nm scale, a 128.30 Ω is shown at a bandwidth of 1.80 GHz. The 90 nm scale simulation showed a 166.59 Ω at 1.33 GHz, while the 130 nm scale showed a 205.99 Ω at 1.06 GHz.

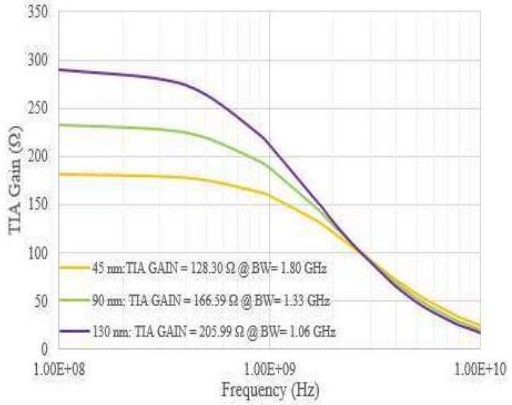


Fig. 7. TIA Gain in Ohm.

In Fig. 8, the input impedance frequency response is shown. For 45 nm scale, a 247.11 Ω is shown at a bandwidth of 1.80 GHz. The 90 nm scale simulation showed a 330.22 Ω at 1.33 GHz, while the 130 nm scale showed a 414.03 Ω at 1.06 GHz.

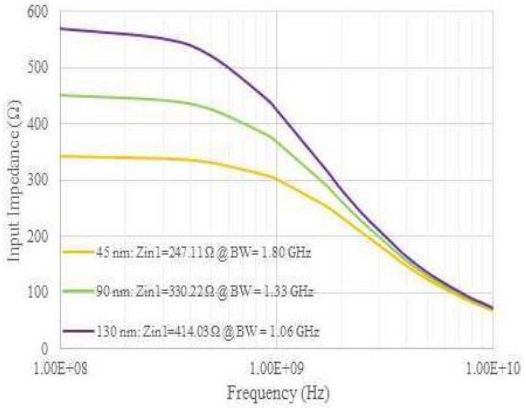


Fig. 8. Input Impedance frequency response.

In Fig. 9, the total power consumption is reported. For the 45 nm scale, a 0.611 mW is shown which represents the sum of power consumption as per each transistor. For the 90 nm scale, a total power consumption of 0.287 mW is manifested, while in 130 nm scale, a total of 0.173 mW is reported.

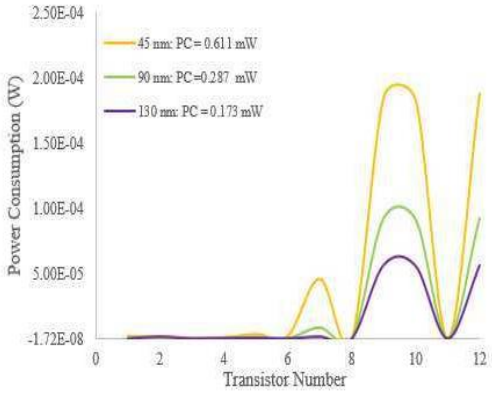


Fig. 9. Power Consumption as per each transistor.

The input referred noise current (spectral density) is simulated in Fig. 10, for 45 nm scale, a 16.35 $pA/\sqrt{Hz}$ is shown at a bandwidth of 1.80 GHz. The 90 nm scale simulation showed a 12.17 $pA/\sqrt{Hz}$ at 1.33 GHz, while the 130 nm scale showed a 10.60 $pA/\sqrt{Hz}$ at 1.06 GHz.

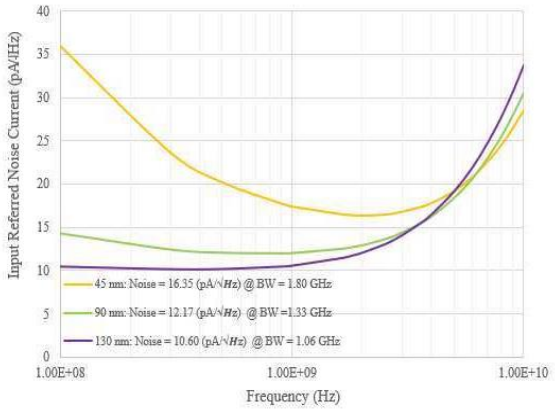
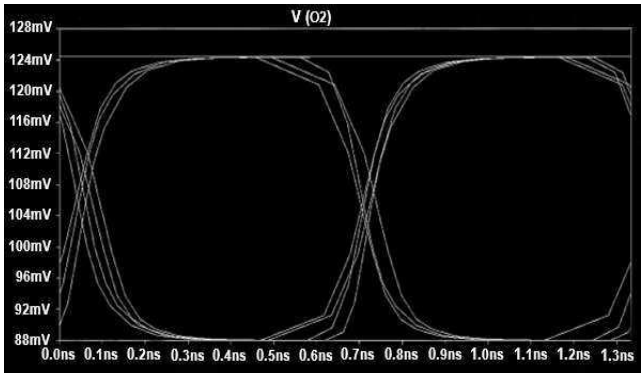


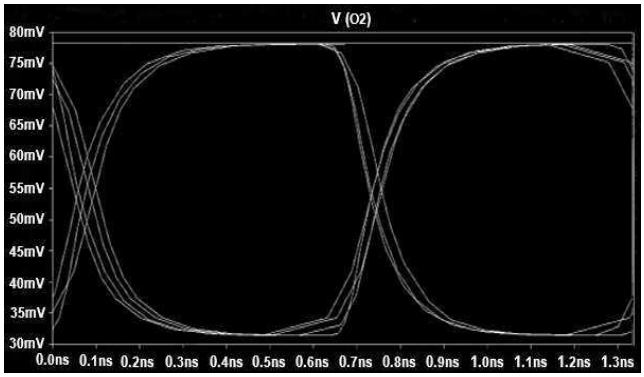
Fig. 10. Input referred noise current spectral density versus signal frequency.

The eye diagram for the 45 nm TIA proposed design is presented in Fig. 11(a). The slope that corresponds to a change in voltage swing of 14.1 mV versus a change of 0.28 ns. This slope is relatively small enough which indicate the sensitivity to timing error. The measure of jitter is around 0.05 ns and that is expressed as the time variation of zero crossing, while the best time to sample is around 0.62 ns defined as the decision point in which the most open part of the eye is equivalent to the best signal-to-noise "S.N.R.," ratio. The "S.N.R.," ratio at the sampling point is equivalent to 18.8 mV. As in the 90 nm scale for the same TIA topology Fig. 11(b), the slope that corresponds to a change in voltage swing of 23.2 mV versus a change of around 0.43 ns. The measure of jitter is around 0.047 ns, while the best time to sample is around 0.63 ns. The "S.N.R.," ratio at the sampling point is equivalent to 24.5 mV. Regarding the 130 nm scale for the same TIA topology Fig. 11(c), the slope that corresponds to a change in voltage swing of 27.6 mV

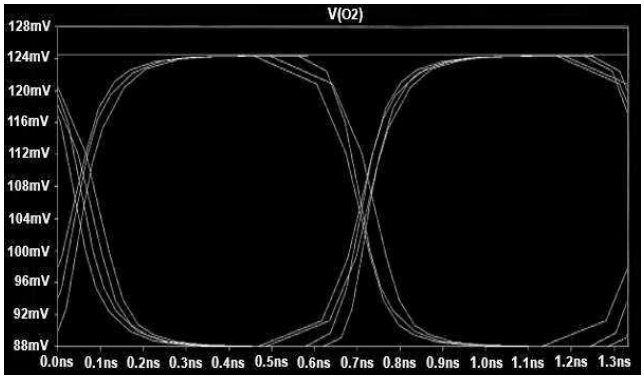
versus a change of around 0.6 ns. The measure of jitter is around 0.02 ns, while the best time to sample is around 0.63 ns. The SNR ratio at the sampling point is equivalent to 30.5 mV. Given that the eye opening occurs 'vertically and horizontally' as in Fig. 11 and due to the bandwidth series (1.80 GHz, 1.33 GHz and 1.06 GHz), it is fair to say that there will be a very limited Inter Symbol Interference "I.S.I.," in random data. For the sake of comparative performance, a 1.5 Gb/s input bit sequencing was applied despite lower bandwidths at 90 nm and 130 nm scales that correspond to 1.33 GHz and 1.06 GHz respectively.



(a) 45 nm scale.



(b) 90 nm scale.



(c) 130 nm scale.

Fig. 11. Eye diagram by bit sequencing at 1.5 Gb/s.

In comparative performance for the 45 nm scale as in Table I, it appears that the trade-off in TIA gain, bandwidth and input referred noise is in line with other literature. In given literature, the lowest possible power consumption is 0.01 mW [2], however, the dc supply voltage is not specified as TIA gain, bandwidth and input referred noise current spectral density are 140 dBΩ, 10 MHz and 4.6 $pA/\sqrt{Hz}$ respectively, while in this work they are 42.16 dBΩ, 1.80 GHz and 16.35 $pA/\sqrt{Hz}$ respectively. This contrast in data appears to be application-specific. Comparing power consumption with other values [1,13], the level of 0.611 mW can be competitive in various cases despite the 1.80 GHz level of f_{-3dB} bandwidth despite that the level of 42.16 dBΩ in this work is moderately lower from application point of view.

TABLE I

COMPARATIVE PERFORMANCE WITH OTHER LITERATURE FOR 45 NM SCALE

Ref.	[1]	[13]	[2]	**This Work**
Year	2012	2018	2022	**2023**
CMOS Technology	45 nm	45 nm	45 nm	**45 nm**
TIA Gain (dBΩ)	7.6	74.4	140	**42.16**
Bandwidth (GHz)	33	23	10 MHz	**1.80**
Input Referred Noise ($pA/\sqrt{Hz}$)	20.5	12	4.6	**16.35**
Power Consumption (mW)	9	36.6	0.01	**0.611**
dc Supply Voltage (V)	1	1	-	**1**

In Table II, there is a clear convergence between this work with given literature [14-16] in terms of TIA gain. There is an indirect relationship between power consumption and bandwidth given the TIA gain trade-off with bandwidth. The 0.287 mW level of power consumption in this work is near 4 times lower than that of comparative literature [16]. However, the f_{-3dB} bandwidth in the indicated literature is near 5 times higher with closer results in TIA gain and input referred noise given that a 1.2V of dc supply voltage is applied.

TABLE II

COMPARATIVE PERFORMANCE WITH OTHER LITERATURE FOR 90 NM SCALE

Ref.	[14]	[15]	[16]	**This Work**
Year	2019	2020	2021	**2023**
CMOS Technology	90 nm	90 nm	90 nm	**90 nm**
TIA Gain (dBΩ)	50.5	41	39.8	**44.34**
Bandwidth (GHz)	7.3	6.5	24.8	**1.33**
Input Referred Noise ($pA/\sqrt{Hz}$)	13.7	33.4	50	**12.17**
Power Consumption (mW)	1	1.67	11.6	**0.287**
dc Supply Voltage (V)	1.2	1	-	**1**

The same approach is followed in Table III in which there are some divergent results between this work and given literature [17-18] in terms of TIA gain and given the compromise in having as low as 0.173 mW (this work) of power consumption, this divergence is expected. However, it important to see that 1.5V of dc supply budget is applied [18] compared to 1V in this proposed TIA topology. A drawback of high levels of power consumptions are reported in these literatures with an advantage of wider bandwidths. The high-power consumption within the stated literature

[17] with 3.3V supply voltage constitutes a considerable separation from this work. With no indication of dc supply voltage [6] compared to this work, a 300 mW versus 0.173 mW constitute a huge difference, however, TIA gain and bandwidth are higher in comparison.

TABLE III

COMPARATIVE PERFORMANCE WITH OTHER LITERATURE FOR 130 NM SCALE

Ref.	[17]	[18]	[19]	**This Work**
Year	2019	2019	2021	**2023**
CMOS Technology	130 nm	130 nm	130 nm	**130 nm**
TIA Gain (dBΩ)	59.885	71	66	**46.25**
Bandwidth (GHz)	6.9	31	40	**1.06**
Input Referred Noise ($pA/\sqrt{Hz}$)	7.925	14.5	9.4	**10.60**
Power Consumption (mW)	0.872	300	142	**0.173**
dc Supply Voltage (V)	1.5	-	3.3	**1**

Based on the above comparative performance tables, a data table is formed that includes all parameters with relevant literature that reported the best performance (with 45 nm, 90 nm and 130 nm scale) regarding low power consumption and input referred noise current (spectral density) and that is part of the main focus of this work as shown in Table IV. This work still in the lead for applications that require low power consumption and input referred noise current spectral density. For applications that require extremely low magnitudes of power consumption as in 0.01 mW [2], a low bandwidth of 100 MHz limits the application demand to a considerable extent.

TABLE IV

DATA TABLE FOR ALL RELEVANT PARAMETERS BASED ON 45 NM, 90 NM AND 130 NM SCALES WITH BEST PERFORMANCE

Ref.	[2]	[14]	[17]	**This Work**
Year	2022	2019	2019	**2023**
Channel Length (nm)	45	90	130	**45 nm** **90 nm** **130 nm**
Input Referred Noise $(pA/\sqrt{H_z})$	4.6	13.7	7.925	**16.35@45nm** **12.17@90nm** **10.60@130nm**
Power Consumption (mW)	0.01	1	0.872	**0.611@45nm** **0.287@90nm** **0.173@130nm**
TIA Gain (dBΩ)	140	50.5	59.885	**42.16@45nm** **44.34@90nm** **46.25@130nm**
Bandwidth (GHz)	100 MHz	7.3	6.9	**1.80@45nm** **1.33@90nm** **1.06@130nm**
DC Supply Voltage (V)	-	1.2	1.5	**1**
Input Capacitance	1 pF	200 fF	200 fF	**100 fF**

IV. DISCUSSION

With regard to the RGC input stage, despite the limited CS voltage gain as indicated in $g_{m2} \cdot (r_{O9} \| r_{O2} \| r_{O4})$, a low input impedance was possible to achieve despite the low supply voltage of 1V. From the current gain of "(3)," a zero pole comes from the local feedback path, this pole is the time constant at node a. A unity current gain is achieved at low frequency, however, as frequency is increased, the current gain drops in response. In addition, the Miller capacitance C_{ab} lowers the gain of the local feedback by $(1 + g_{m1} r_{O8})$ at higher frequencies and that can lower virtual ground effect at input node $in1$.

Within the CG-CS subsequent stage, the low input impedance of the CG core (ignoring high CS input impedance) enables wider bandwidth of the CG-CS topology that accommodates the time constant of the output node O_1 from the RGC input stage. Combinational CG-CS output impedance is determined by how low is the output conductance of transistor M_{10}. Since, the output resistances of transistors M_5 and M_6 are high enough, it was not possible to neglect channel length modulation. The CG stage on its own suffers from a trade-off problem between gain and overdrive voltage, however, the drain resistance of transistor M_5 is high enough to achieve a considerable voltage gain.

Theoretically, CS configurations represented by transistors M_1, M_2, M_5 and M_6 (having M_2 and M_5 being also in CG topology at time and phase shifts with CS outputs), they draw no current at inputs and therefore have an extremely high input impedances and current gains. The mentioned high input impedances force the input signal to converge at the CG input nodes $in1$ and $in2$ with impedances of $1/g_{m2}$ and $1/g_{m5}$ which are extremely low, hence enabling transistors M_2 and M_5 to conduct with wide bandwidth. The level of high current gain serves the output of RGC input stage (being a current gain provider) as well as it serves to stabilize drain current path when it comes to the CG output nodes for transistors M_2 and M_5.

The channel length variation from 45 nm towards 90 nm and 130 nm have major effects on the proposed TIA performance in terms of gain (in dBΩ and in Ω) as in Fig. 6 and Fig. 7 respectively. To simplify this concept, the CS configuration of transistor M_1 in Fig. 2 enables the fact that the channel length modulation parameter λ does have an inverse relationship with channel length $\lambda \alpha L^{-1}$ leading to have the voltage gain $A_v \alpha L$ to be proportional to channel length in nonlinear manner. Since the TIA gain is proportional to voltage gain, it is fair to assume that it is also proportional to channel length L. It is important to point out that both input stage and subsequent CG-CS stage are based on the behavior of a CG and a CS configuration. Both configurations do exhibit near identical small signal equivalent circuit model, so understanding above parameters change in terms of transistor M_1 within the input stage should clarify the case especially that transistor M_1 is configured in a CS topology at input node $in1$ (mentioned earlier) as well as having transistor M_2 in CG topology from node b stand point.

The channel length variation does also have considerable influence on f_{-3dB} bandwidth. Since the dc input resistance R_{in1} is determined by its inverse relation with r_{O8} significantly as $r_{O8} \alpha L$, then from CS point view, the dc input resistance R_{in1} is inversely proportional to channel

length L, therefore, as channel length moves up from 45 nm towards 130 nm, the dc input resistance goes up and subsequently the input impedance Z_{in1} frequency response develops as in Fig. 8.

So far as power consumption is concerned, it is all down to output resistance r_{o8} of a particular transistor within the proposed TIA topology. Given that $r_O = 1/(\lambda I_D)$ while r_O is proportional to L as $\lambda \alpha L^{-1}$, it is valid to say that 130 nm transistor structure will consume less power than the 45 nm one as r_O is in an inverse relationship with drain current I_D where power consumption= $I_D V_{DD}$ for a particular transistor as in Fig. 9.

With regard to input referred noise current spectral density versus series channel lengths (from 45 nm upwards till 130 nm), according to "(20)," and as $\overline{i^2}_d = \gamma 4kTg_m$, the mean square channel thermal noise current (spectral density) at the drains of transistors M_1, M_2, M_3 and M_8 are dominated by transconductances parameters g_{m1}, g_{m2}, g_{m3} and g_{m8} respectively which are in an inverse relationship with channel length, then it is obvious that the 130 nm scale will register the lowest level of input referred noise current compared to 45 nm and 90 nm scales as in Fig. 10.

There is a hidden challenge related to the trade-off compromise in TIA gain versus bandwidth and noise. Originally and without channel length variation, the problem of dc supply voltage limit remains the main obstacle. For instance, the RGC TIA input stage became an option since a voltage headroom for two gate-to-source voltages was accommodated. These voltages did not exceed the 1V supply limit when transistors M_1 and M_2 are biased at just below half of the supply limit for instance. It means that transistors biasing can be lowered to fit in the 1V supply limitation without slowing down the RGC topology speed considerably. The RGC input stage topology was more suitable as a series of channel lengths (from 45 nm up to 130 nm) enabled an efficient 1V supply voltage utilization. This channel length variation addressed this obstacle with significant channel length range.

The trade-off in gain versus bandwidth and input referred noise current for a series of channel lengths conforms to the same trade-off behavior for a single channel length. In other words, the effect of channel length series variation on above trade-off can be equivalent to that of channel length modulation given that the output resistance $r_O = 1/(\lambda I_D)$ where λ is the channel length modulation parameter. Trade off consistency shows that the short channel effect in terms of Drain-Induced Barrier Lowering "D.I.B.L.," did not seem to have much of an impact as the drain-to-source depletion region overlap for a particular transistor could have been minimal to a greater extent. It means that the bottleneck regarding.

V. Conclusion

The trade-off in gain versus bandwidth and input referred noise current still applies when channel length is moved upwards from 45 nm towards 130 nm. In addition, a considerable reduction in power consumption and input referred noise current using the proposed topology was achieved especially when channel length is increased. A transimpedance amplifier gain series (42.16 dBΩ, 44.34 dBΩ and 46.25 dBΩ) that correspond to the series (1.80 GHz, 1.33 GHz and 1.06 GHz) of f_{-3dB} bandwidths is reported corresponding to the channel length series (45 nm, 90 nm and 30 nm) with an input referred noise current spectral density series (16.35 pA/$\sqrt{\text{Hz}}$, 12.17 pA/$\sqrt{\text{Hz}}$ and 10.60 pA/$\sqrt{\text{Hz}}$) of reduction. Furthermore, a power consumption reduction occurred as channel length is moved upward for the same proposed topology. A total power consumption series (0.611 mW, 0.287 mW and 0.173 mW) was reported that corresponds to the reported channel length series. A future work may involve the replacement of PMOS current sources with active inductor configuration that may contribute to lower power consumption given its extremely high impedance expected at over 1 GHz signal frequency.

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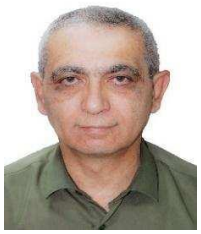

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