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Effect of Oxide Thickness on GaN-based Double Gate MOSFETs

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***Abstract*—- The effect of oxide thickness (EOT) on GaN-based double gate (DG) MOSFETs have been explored for low power switching device. The gate length (LG) of 8 nm with 4 nm underlap is considered. The device is turned off and on for gate voltage (VGS) of 0 V and 1 V, respectively. The effective oxide thickness (EOT) is varied from 1 nm to 0.5 nm and the device performance is evaluated. For EOT = 0.5 nm, the OFF-state current (IOFF), subthreshold slope (SS) and drain induced barrier lowering (DIBL) are obtained 2.97×10-8 A/µm, 69.67 mV/dec and 21.753 mV/V, respectively. These results indicate that, it is possible to minimize short channel effects (SCEs) by using smaller value of EOT.**

Keywords— Drain-induced barrier lowering (DIBL); Effective Oxide Thickness (EOT); GaN; OFF-state current (IOFF); Subthreshold slope (SS);

I. INTRODUCTION

Switching is the most important phenomenon for future device [1-3]. In order to, keep pace with the miniaturization standards, the feature size of MOSFET has been scaled down obeying Moore's law [4], which has started with 10 µm half-pitch of a standard memory cell in 1971, has reached as low as 14 nm in 2015 [5]. The aim is to reach "more than Moore" according to the ITRS [6]. Scaling of MOSFETs has given rise to the continued improvement in both devices switching speed and density of the CMOS technology. However, they are now about to reach their physical limit [7-9]. Due to continue scaling, problems such as the short-channel effect (SCEs), parasitic capacitance, leakage current etc. arose. Double-gate MOSFETs [10] has shown superior performance in comparison to conventional single gate MOSFETs for minimizing these problems. DG MOSFETs has high transconductance and near ideal sub-threshold swing. The two gates provide good electrostatic integrity. Therefore, reduces SCEs and improve control over channel [11-14]. Silicon (Si) is the central material for the electronic devices for the last three decades. Over the years, most of the works carried out on conventional Si-based DG MOSFET [15-18]. However, as the devices getting smaller Si-based DG MOSFET has reached to its performance saturation faces many challenges [19-21]. GaN is a probable candidate for DG MOSFETs [22-23] due to its low effective mass and wide bandgap [24-25], which leads to high mobility and high saturation velocity than Si. Therefore, it is possible to fabricate high-speed, high performance devices using GaN-based DG MOSETs.

In our previous work with GaN-based DG-MOSFET, it is reported that it's possible to attain the subthreshold slop (SS) of 62.90 mV/decade and drain induced barrier lowering (DIBL) of 33.59 mV/V by optimizing the symmetrical underlap length with a constant gate length (LG) 12 nm [26]. The effective oxide thickness (EOT) is also another key parameter to control the OFF-state condition for future low power logic switching devices. There are some previous works that based on effect of oxide thickness [27 -28]. However, there is no report on variation of EOT for GaN-based DG-MOSFETs. Therefore, more theoretical works are immense importance.

In this paper, the effect of oxide thickness on device performance has been evaluated. EOT is varied from 1 nm to 0.5 nm for device with channel length (LCH) 12 nm and gate length (LG) 8 nm i.e. device with 4 nm gate underlap. The purpose of this is to find out the optimized value of EOT, that provides better device performance.

II. DEVICE STRUCTURE AND SIMULATION METHODOLOGY

The schematic structure of GaN-based DG-MOSFET is shown in Fig. 1. The channel length (LCH) is considered 12 nm. The supply drain voltage (VDD), channel doping, and body thickness (tbody) employed throughout this paper is considered as 1 V, 1×1017 cm-3 and 5 nm, respectively. The source to gate length (LGS) and gate to drain length (LGD) is considered as 3 nm in both cases. The doping of both source and drain regions is considered as 1×1020 cm-3. The Hafnium dioxide (HfO2) is employed as dielectric under the both top and bottom gates. According to the value of effective oxide thickness (EOT) the thickness of HfO2 (tin) is adjusted. At first, 4 nm of gate underlap is introduced by keeping the LCH constant at 12 nm and the gate length (LG) 8 nm for an EOT of 1 nm. Then EOT is varied from 1 nm to 0.5 nm and results are evaluated.

The mesh structure is shown in figure 2. For all the simulation, the spacing in the x-axis is considered 0.25 nm and in the y-axis it is considered 0.1 nm. Along each vertical slice located at the horizontal position of x, 1-D Schrodinger

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equation is solved. All calculations are done at room temperature, T = 300 K. The non-equilibrium Green's function (NEGF) method in mode space approach has been incorporated using SILVACO ATLAS.

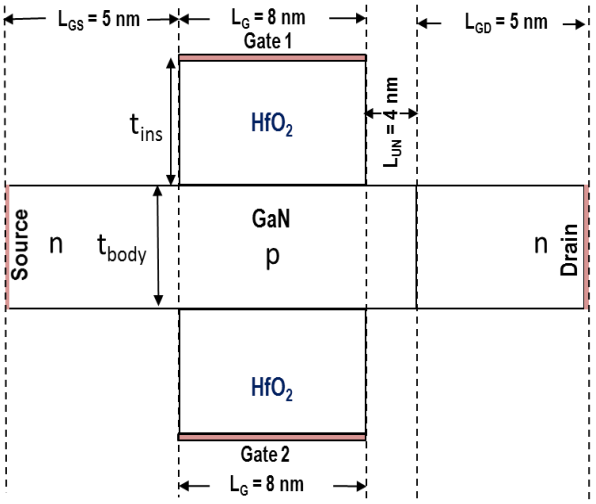

Fig. 1. Schematic structure of GaN-based DG-MOSFET.

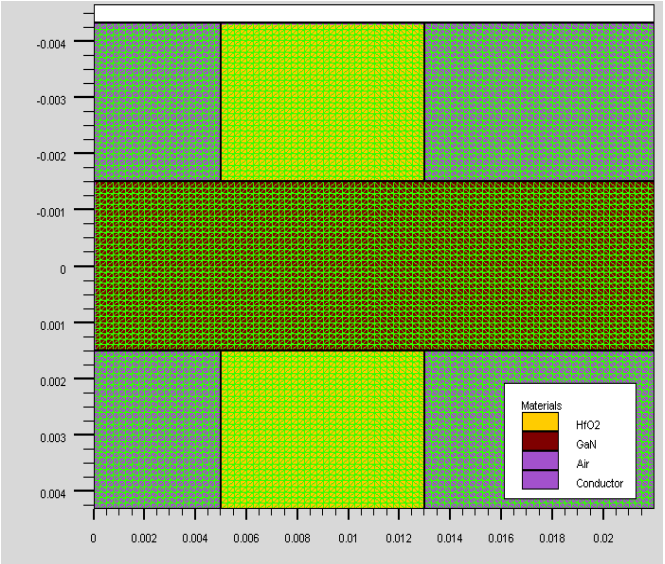

Fig. 2. Mesh Structure of GaN-based DG-MOSFET.

III. Results and Discussions

In this paper, at first, the device performances have shown for a gate underlap of 4 nm i.e. L_{CH} = 12 nm and L_G = 8 nm, where EOT is considered 1 nm. Then keeping L_{CH} and L_G fixed at 12 nm and 8 nm, respectively, EOT is varied from 1 nm ~ 0.5 nm and the device performance are analyzed.

The conduction band profile for gate underlap 4 nm and EOT 1 nm is shown in figure 3. In fig. 3 (a) the band profile is shown for OFF-state condition. In OFF-state condition the gate to source voltage (VGS) is applied 0 V. Therefore, no change in the top of the barrier of the conduction band and it remains high. As the VGS is increased to 1 V for ON-state condition the barrier height is decreased and more electron flows through the channel. Therefore, the MOSFET is in ON-state.

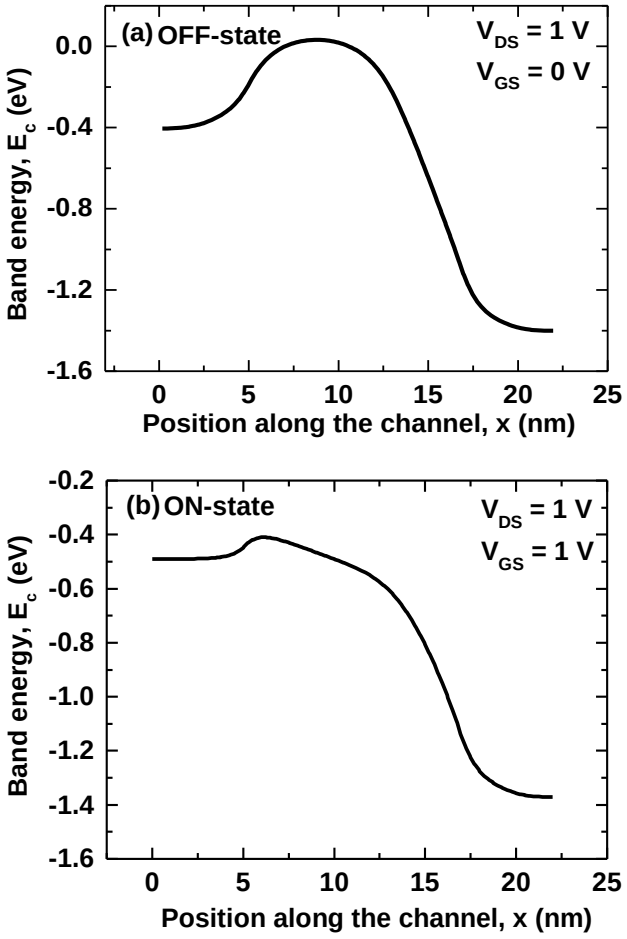

Fig. 3. Band profiles for LG = 8 nm in the (a) OFF-state at VDS = 1 V and VGS = 0 V (b) ON-state at VDS = 1V and VGS = 1V.

The transfer characteristics curves have been shown in the Fig. 4 for different drain voltage (VDS) of 1 V and 0.05 V. As the drain voltage increases the ON-state current increases.

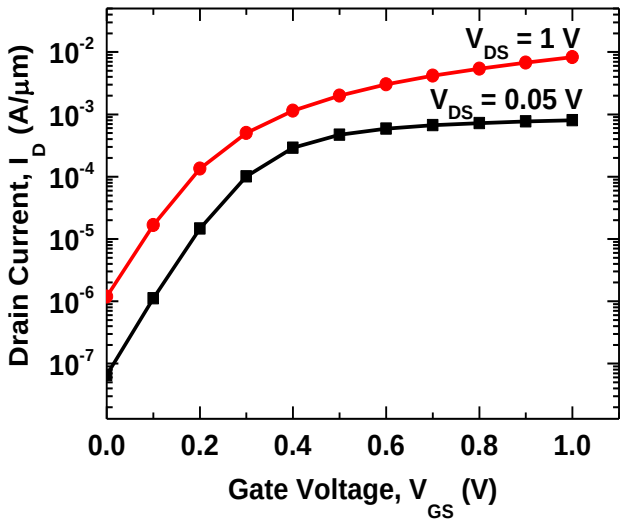

Fig. 4. Transfer characteristics curve

In Fig. 5, the dc characteristic curve is shown. With the increase of VGS, the drain current (ID) increases. The highest ID of 8.29 mA/μm is obtained for VGS = 1 V and VDS = 1 V, which is considered as ON-state current.

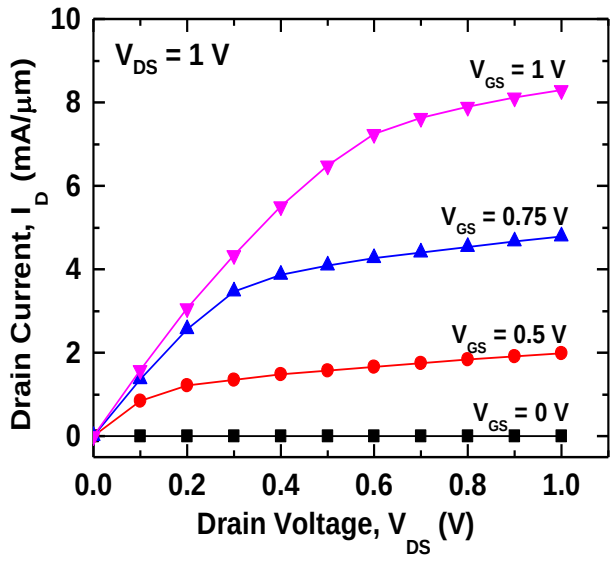

Fig. 5. Output characteristic curve for different V_{GS}.

Electric field concentration is shown in Fig. 6 (a) and (b) for OFF-state and ON-state. From the figure, it can be observed that during OFF-state condition there is no change in electric field in the channel region as no current is flowing through the channel.

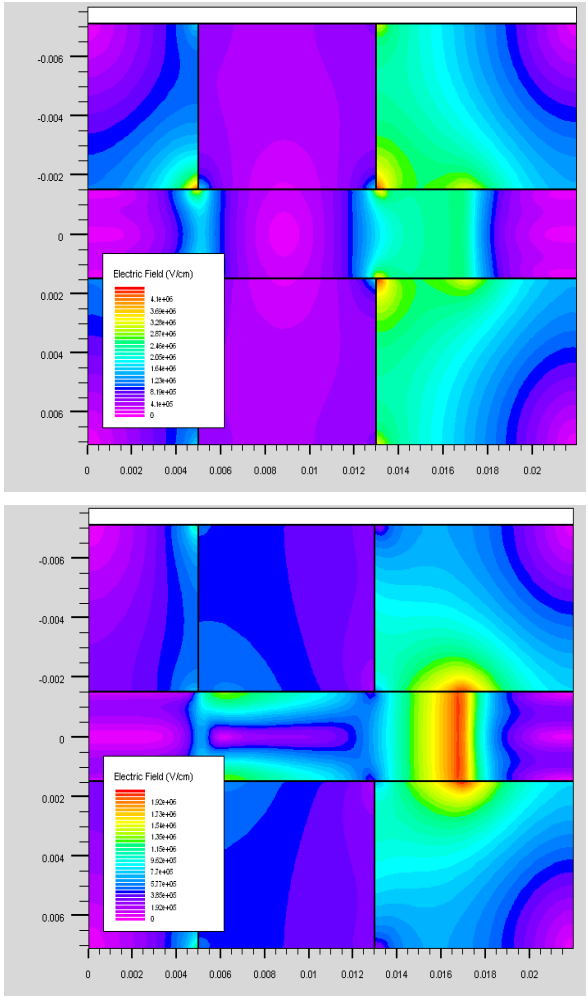

Fig. 6. Electric Field Contour (a) OFF-state condition (b) ON-state condition.

However, as the device turned on a change in electric field is observed in both top and bottom of the channel. Due to double gate two channels are created on the top and bottom of the device and due to the current flow in these channels electric field is increased in these regions.

Subthreshold slope (SS) means how much mV increases in gate voltage does it take to increase the output current by a factor of 10. Equation 1 describe the definition of SS. The ideal value for SS is 60 mV/decade. The value of SS is found 87.27 mV/decade for the device.

$$SS = \frac{\Delta V_G}{\Delta \log I_D} \quad \ldots (1)$$

The DIBL can be expressed as the translation of threshold voltage due to the change in drain to source voltage, as shown in equation 2. The value of DIBL is found 114.08 mV/V for device with 4 nm underlap.

$$DIBL = \left[\frac{V_{TH1} - V_{TH2}}{V_{DS1} - V_{DS2}} \right] \quad \ldots (2)$$

The static power consumption for the device with EOT 1nm is found 1.193×10^{-6} W/μm.

A. *Effect of oxide thickness*

In the previous part, it described about the result for device with gate underlap 4 nm and EOT 1nm. This part of the paper focused on the device performance based on EOT. Therefore, considering the device with gate underlap, the EOT is varied from 1 nm ~ 0.5 nm. The relation of oxide thickness with EOT is given by equation 3. The objective of presenting these results is to determine the optimized EOT value for the device

$$t_{ins} = \frac{k_{HfO_2}}{k_{SiO_2}} \times EOT \quad \ldots (2)$$

where, k_HfO2 and k_SiO2 are the di-electric constant of HfO2 and SiO2.

In Fig. 7 (a) and (b) the conduction band for OFF-state and ON-state is shown. From the figure, it is observed that during OFF-state the barrier height is higher for smaller EOT (0.5 nm). With the increase of EOT barrier height decreases. Therefore, for small EOT value, OFF-current is lower. Lower EOT means there is a less possibility of tunneling and leakage current. During ON-state, the barrier height is lower at a smaller value of EOT (0.5 nm). When oxide thickness is thin the gate voltage has a greater effect on the top of the barrier. Therefore, the barrier is lower for small EOT value.

The main effect of EOT on device performance is on OFF-state condition. As the value of EOT is decreased, the OFF-current improves. Therefore, ION¬/IOFF ratio increases. ION¬/IOFF ratio has a significant effect on device power consumption. Hence, smaller EOT means low power consumption. In Fig. 8 the variation of ION/IOFF ratio with EOT value is shown. The highest value of ION¬/IOFF ratio (3.09×105) is obtained for 0.5 nm EOT.

The dependency of SS on EOT is shown in Fig. 9. With the decrease of EOT, SCEs become prominent so that SS decreases considerably. The lowest value of SS (~ 69.67 mV/decade) is obtained for EOT = 0.5 nm.

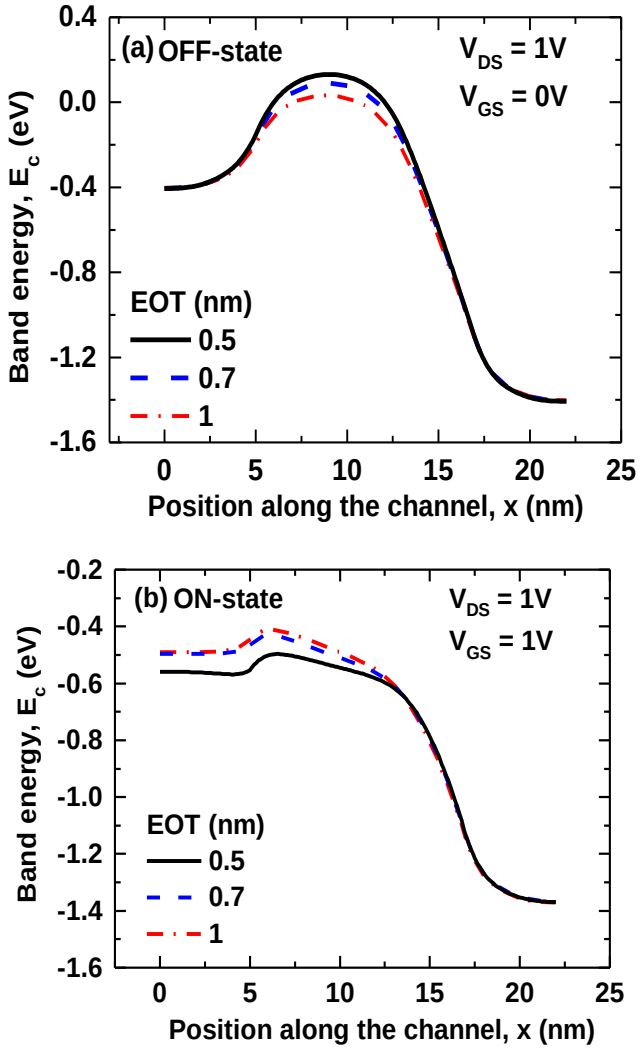

Fig. 7. Band profiles for different EOT in the (a) OFF-state at VDS= 1V and VGS = 0V (b) ON-state at VDS = 1V and VGS = 1V

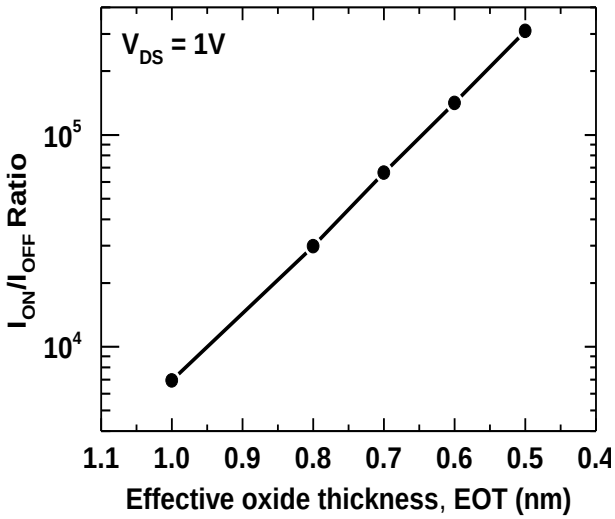

Fig. 8. Variation of ION/IOFF ratio with EOT value

In the Fig. 10, it is shown the variation of DIBL with respect to EOT. An increase in EOT increases the effect of drain potential on channel and gate losses control over the channel. Therefore, DIBL value is increased. The lowest value of DIBL (~ 21.753 mV/V) is found for EOT 0.5 nm.

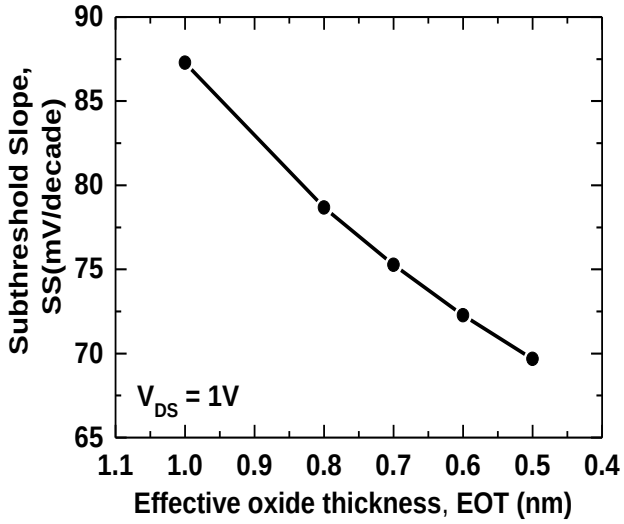

Fig. 9. Variation of SS with EOT value.

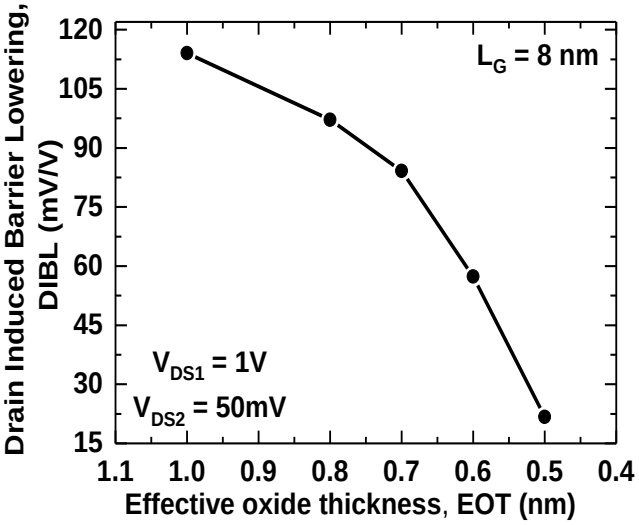

Fig. 10. Variation of DIBL with EOT value

In the Fig. 11, it is shown the variation of threshold voltage with respect to EOT. An increase in EOT decrease the threshold voltage means the OFF-state condition deteriorate. Therefore, 0.5 nm EOT is better for the devices.

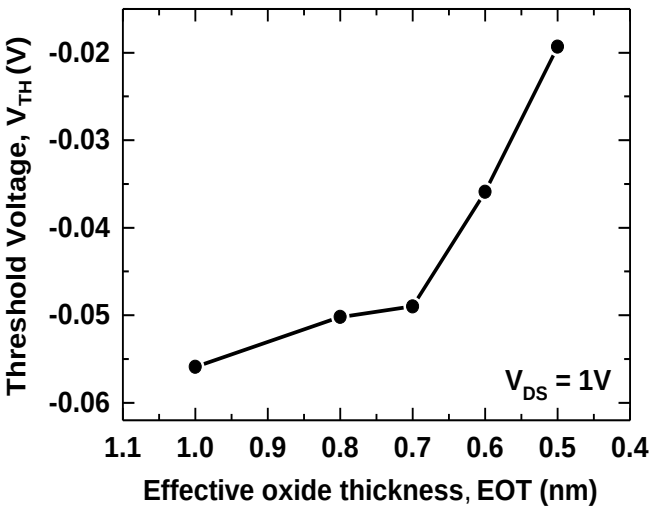

Fig. 11. Variation of threshold voltage with EOT value.

In the Fig. 12, the electric field (EF) for different EOT value has been shown. The dashed line indicates the OFF-state (VGS = 0 V) and the solid line indicates the ON-state (VGS = 1 V). It can be determined from the figure that as the EOT value decreased from 1 nm to 0.5 nm the value of EF is increased. There is a higher peak on the drain side for 0.5 nm EOT at ON-state. The peak of EF near the drain end results in electrons entering the channel with a low initial velocity, gradually accelerating toward the drain. The maximum electron velocity is reached near the drain. Therefore, suppressing the SCEs.

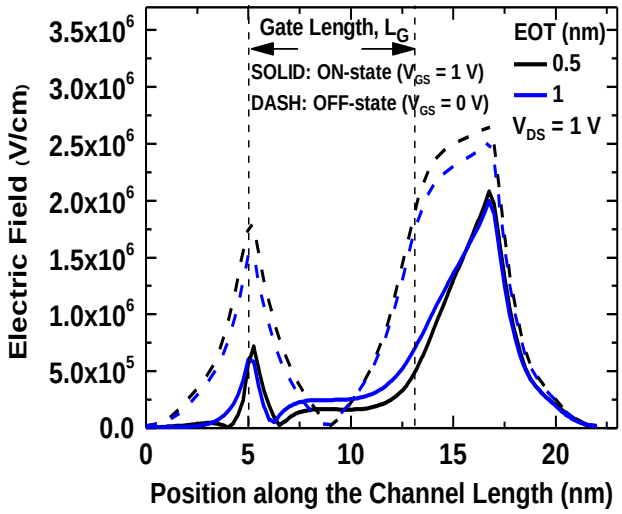

Fig. 12. Electric Field for different EOT values.

In the fig. 13, the surface potential for different EOT has been shown. As the value of EOT decreases from 1 nm to 0.5 nm the value of potential increases in the channel region. Therefore, the gate potential has more control over the channel for smaller EOT. Therefore, DIBL decreases for lower EOT and the OFF-state current decreases. Which leads to suppress in the SCEs.

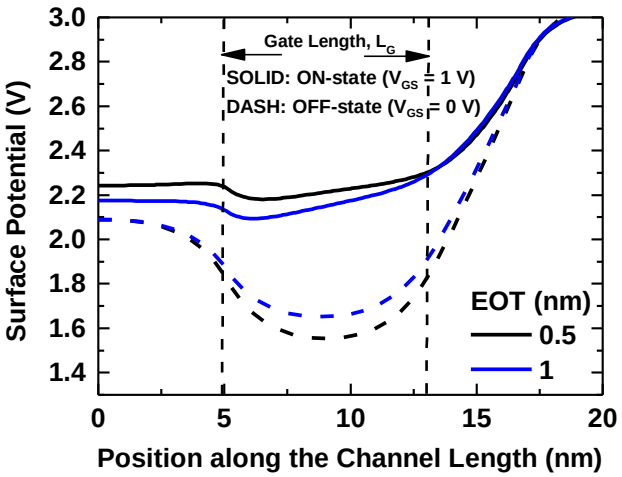

Fig. 13. Surface Potential for different EOT values.

Static Power dissipation is a significant parameter for CMOS technology. In Fig. 14 variation of static power dissipation ($I_{OFF}.V_{DD}$) with respect to EOT has been shown. From the figure it can be obsereved that, due to the increase of I_{OFF} with EOT the power dissipation also increases. Lowest power dissipation value (~ 2.97 $\times 10^{-8}$ W/μm) is obtained for EOT = 0.5 nm. A lower static power is highly desirable for low power and high-performance logic applications. Therefore, 0.5 nm EOT is appropriate to design devices that required lower power consumption.

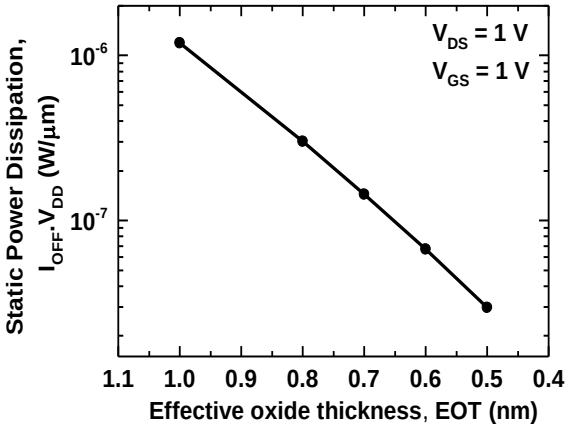

Fig. 14. Static power dissipation for different EOT values.

IV. Conclusions

The effect of oxide thickness on GaN-based Double Gate MOSFETs has been shown with simulated results. Introducing gate underlap of 4 nm, with fixed EOT (1 nm) the device performances are evaluated. Then, for the that device, EOT is varied from 1 nm to 0.5 nm. The purpose is to find out the optimized value of EOT for the device. From the results, it is determined that, with the increase of EOT the SCEs become prominent. Therefore, to minimize the SCEs and improve OFF-state condition in future small devices, smaller values of EOT is desired.

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