

Fig.3. Circuit Diagram of simple inverter circuit.

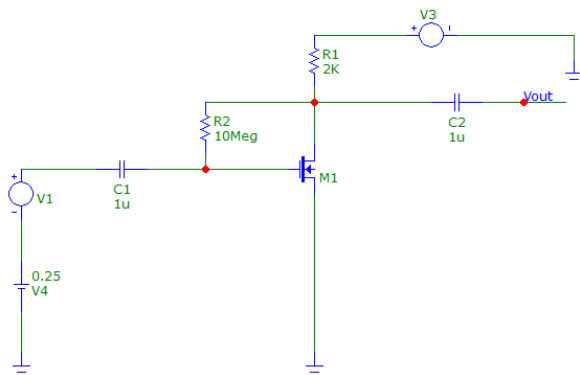


Fig. 4. Self-biasing circuit for frequency response analysis.

The inverter circuit shows accurate results, providing 0V at the output when input is given as 1V and vice-versa. Figure 5 shows the output of the inverter circuit for both models.

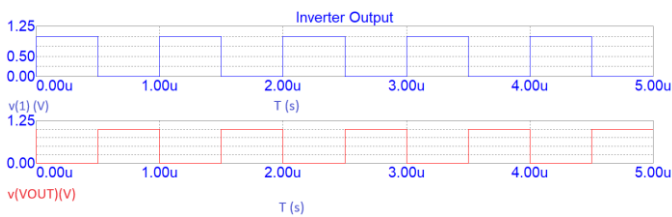
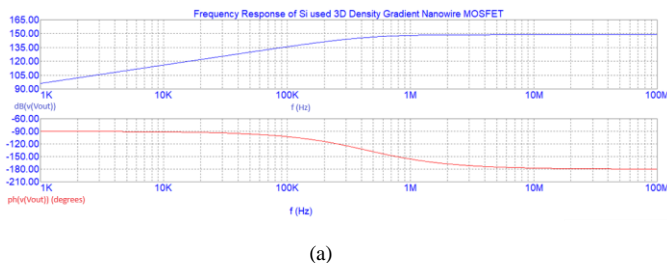
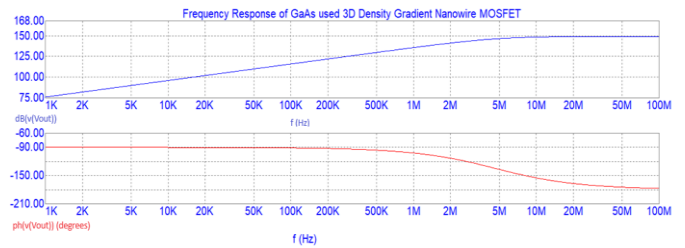


Fig. 5. Inverter circuit output of both Si and GaAs used models.

Lastly, the frequency response curve in dB and phase change curve have been generated for both models. The results are shown in Figures 6 (a) and (b).



(a)



(b)

Fig.6. (a) Frequency response curve of Si used model. (b) Frequency response curve of GaAs used model.

From Figure 6 (a) and (b), the used model has a cut-off frequency at 1MHz while that of the GaAs used model is at 10MHz.

Si has been there since the start as a major material in the semiconductor industry. However, with the reduction in the size of the devices, few limitations are coming up and researchers are going for newer materials to take the place of Si. From the analytical results, it can be said that GaAs can be a better material, impacting the performance and features of devices in the semiconductor industry.

#### V COMPARISON WITH PREVIOUS WORKS

A comparison table has been shown for differentiating the designed model from available research papers. The comparing parameters have been limited to the channel length, oxide thickness, and threshold voltage.

TABLE IV. COMPARISON WITH PREVIOUS WORKS

Research Works	Channel Length[nm]	Oxide Thickness [nm]	Threshold Voltage [V]
[19]	30000	7	0.125
[20]	10	3-10	0.2
[21]	7-10	2.82	0.7
[6]	4	0.8	0.7
Designed Model	3.2	0.5	0.7

Table IV shows that the value of threshold voltage increases with the decrement of channel length and oxide thickness. Moreover, the designed model has the lowest values of channel length and oxide thickness among the mentioned papers.

#### VI CONCLUSION

The paper analyzes the impact of semiconductor materials in designing the 3D density gradient nanowire MOSFET. The models having the same channel length and oxide thickness of 3.2nm and 0.5nm, respectively, have been designed using varied materials, namely Si and GaAs.  $I_d-V_g$ ,  $I_d-V_d$ , gm- $I_d$  curves, and the electron concentration along the x and z coordinates have been analyzed and compared. The analysis showed the drain current, potential-well depth, and transconductance values are higher by approximately  $10^4$ , and almost double in range, respectively, in the case of the

model designed using GaAs as a material compared to the Si-used model. The higher drain current can provide switching losses, which can be controlled if kept within a safe operating area. In addition, a higher drain current is suitable for application in analog circuit designs like amplifiers. Moreover, the extracted data have been utilized to generate model and library files to create a component model. A simple inverter circuit and biasing circuit have been designed with the models to get a digital application-level comparison. The inverter circuit worked accordingly, and the frequency response curve provided the cut-off frequency of both models. It is found that the Si-used model has a cutoff frequency of 1MHz while that of the GaAs-used model is 10MHz, which means the used model can provide faster performance. So, it can be said that the GaAs used model can offer faster performance and more energy than the Si one. From the theoretical and analytical comparison from analysis to application level, it can be concluded that the model using GaAs as the material would give better and faster performance than the model using Si material. Further work might include designing low-power analog application circuits to get analog application-level analysis of the designed nanowire MOSFET.

#### REFERENCES

[1] M.G. Ancona, "Density-gradient theory: a macroscopic approach to quantum confinement and tunneling in semiconductor devices," *J. Comput. Electron.*, vol. 10, p. 65, 2011

[2] S. Jin et al., "Simulation of Quantum Effects in the Nano-scale Semiconductor Device," *J. Semicond. Tech. Sci.*, vol. 4, no. 1, p. 32, 2004.

[3] S. C. Jain et al. Modified Simple Expression for Bandgap Narrowing in N-type GaAs. *Solid-State Electronics* Vol. 35, No. 5, pp. 639-642, 1992.

[4] Jing Wang et al. A three-dimensional quantum simulation of silicon nanowire transistors with the effective-mass approximation. *Journal of applied physics* volume 96, number 4 15 August 2004.

[5] Yiming Li et. al. Computer Simulation of Germanium Nanowire Field Effect Transistors. National Science Council (NSC) of Taiwan. 2004-2005.

[6] A.R. Brown et al., "Comparison of Density Gradient and NEGF for 3D Simulation of a Nanowire MOSFET," *Proc. 2009 Spanish Conf. Elec. Dev.*, p. 140, Feb. 11–13, 2009.

[7] S. Rhee et al. Extension of the Density-Gradient Model to the Second-Order Quantum Correction for Analysis of the Single-Charge Effect in Sub-10-nm MOS Devices. DOI 10.1109/JEDS.2020.2971426, *IEEE Journal of the Electron Devices Society*.

[8] Awanit Sharma, Shyam Akashe. Performance Analysis of Gate-All-Around Field Effect Transistor for CMOS Nanoscale Devices. *International Journal of Computer Applications* (0975 – 8887) Volume 84 – No 10, December 2013.

[9] Mohinder Bassi et al. Analysis and Design of high-K Material Nanowire Transistors for Improved Performance. *IEEE*. 2019.

[10] B.J. Nel et al., A Brief Overview of SiC MOSFET Failure Modes and Design Reliability, *Procedia CIRP*, Volume 59, 2017, Pages 280-285, ISSN 2212-8271, <https://doi.org/10.1016/j.procir.2016.09.025>.

[11] Sasank et. al. Cryogenic Analysis of Junctionless Nanowire MOSFET during Underlap in Lower Technology Nodes. *Journal of Physics: Conference Series*. *Journal of Physics: Conference Series*, Volume 1879, Ibn Al-Haitham International Conference for Pure and Applied Sciences (IHICPS) 9-10 December 2020, Baghdad, Iraq. DOI 10.1088/1742-6596/1879/3/032124.

[12] Jaiswal, S. et al. Digital Performance Analysis of Double Gate MOSFET by Incorporating Core Insulator Architecture. *Silicon* 14, 10977–10987 (2022). <https://doi.org/10.1007/s12633-022-01811-7>.

[13] O. Vicente et al., "Effect of Drift and Diffusion Processes in the Change of The Current Direction in a FET Transistor," 2014.

[14] RF Wireless World. Available at: Microwave semiconductor material-Si, GaAs, InP, GaN, AlN, InN (rfwireless-world.com) [Accessed on 28th September 2022].

[15] Cho et al. (2011). RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs. *IEEE Transactions on Electron Devices*, 1388–1396. (2011). <https://doi.org/10.1109/TED.2011.2109724>.

[16] Dambrine, G. et al. A New Method for Determining the FET Small-Signal Equivalent Circuit. *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES* (Vol. 36, Issue 7). (1988).

[17] Lakrim, A. et. al. The spice dynamic behavioural electrothermal model of silicon carbide power MOSFET. *Journal of Theoretical and Applied Information Technology*. (2016). <https://www.researchgate.net/publication/311268407>.

[18] S. F. Nazreen and M. T. Ali, "Analytical Comparison of the Impact of Si and GaAs as Materials in Designing 3D Density Gradient Nanowire MOSFET for Low Power Applications," 2023 3rd International Conference on Robotics, Electrical and Signal Processing Techniques (ICREST), Dhaka, Bangladesh, 2023, pp. 285-288, doi: 10.1109/ICREST57604.2023.10070082.

[19] S. Sekiguchi et al., "Subthreshold Swing in Silicon Gate-All-Around Nanowire and Fully Depleted SOI MOSFETs at Cryogenic Temperature," *IEEE J. Electron Devices Soc.*, vol. 9, no. December, pp. 1151–1154, 2021, doi: 10.1109/JEDS.2021.3108854.

[20] R. Wang et al., "Analog/RF performance of Si nanowire MOSFETs and the impact of process variation," *IEEE Trans. Electron Devices*, vol. 54, no. 6, pp. 1288–1294, 2007, doi: 10.1109/TED.2007.896598.

[21] S. Ahmed and M. Iktiham Bin Taher, "GaN-based Sub-10 nm Metal-oxide-semiconductor Field-effect Transistors Characterization and Optimization of Novel Two Dimensional Materials for Nonlinear Optics and Ultrafast Photonics Application View project An Evaluation of Financial Performance of Pri," no. April, pp. 25–30, 2016, [Online]. Available: <https://www.researchgate.net/publication/303403319>.



Syeda Fahima Nazreen received her undergraduate degree in Electrical and Electronic Engineering (EEE) from American International University-Bangladesh (AIUB). She received SUMMA CUM LAUDE (Academic Award Based on CGPA) academic distinction at the 20th Convocation Ceremony of American International University-Bangladesh. She has received Deans' List Honor six consecutive times (from Fall 2017 to Spring 2020). She works for Ulkasemi Pvt. Ltd. as an Engineer in the Physical IC Design Department. She has experience in place and route, static timing analysis, power analysis, logical equivalence check, and physical verification from gate-level netlist to GDS in block-level physical IC designing for almost three years. Her research interests are VLSI, IC Design, CMOS circuits, Circuits and Systems, Nanoelectronics, machine learning, and deep learning.



Dr. M. Taseer Ali completed his B.Sc. in Electrical and Telecom Engineering from North South University, Dhaka, in 2007. Then, he pursued higher studies and received an M.Sc. in Communication Engineering with Distinction from Robert Gordon University, Aberdeen, UK, in 2008. He received a full scholarship from the University of Greenwich, London, UK, for the Ph.D.. He completed his doctorate in 2013. Currently, he is working as a Senior Assistant Professor at the Department of EEE, Faculty of Engineering, AIUB, Dhaka. His research interests are in Microwave Circuits and Systems, Antenna Design, Nanoelectronics, CMOS Circuits, VLSI, Analog and Mixed Circuit and IC Design, Quantum Properties of materials, Engineering Education, and Pedagogy.