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Impact of Si and GaAs as Semiconductor Materials: Designing to Application-Level Comparison

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***Abstract*— The semiconductor industry has made life easier by providing many electronic devices. With the advancement of technology, electronic devices need to be updated. This gradual upgrade has led the industry towards nanotechnology. The study aims to provide an analytical comparison from design to application level of the impact of Si and GaAs as semiconductor materials in designing 3D density gradient nanowire MOSFETS. The model has been designed and evaluated based on the characteristics curve and transconductance range. The drain current in the I_d-V_g and I_d-V_d curves for the GaAs-used model is higher than the Si-used model by about 10 times, which is useful for analog applications. The threshold voltage for both models is 0.7V. Besides that, the electron concentration formed a potential well of about 104 for GaAs-used material compared to the model made using Si. In the case of AC analysis, the transconductance range for the model using GaAs is almost double that of the model designed using Si. Later, the extracted data from the curves were utilized to generate model and library files. Finally, an inverter circuit and biasing circuit have been designed with models where the output of the inverter circuit perfectly works. The frequency response curve generated using the biasing circuit showed that the cut-off frequency of the GaAs-used model is 10MHz, whereas it is 1MHz for the Si-used model.**

***Index Terms* — Density gradient, drift-diffusion, semiconductor, nanowire, transconductance, application, inverter, frequency response.**

I. Introduction

THE development of the semiconductor industry takes after Moore's law. The semiconductor industry without transistors cannot even be thought about. With colossal accessibility and capability to fulfill industry necessities, Silicon Material has brought a huge boost to the development of the industry, and it might go along its way for more than 15 years [1]. Alongside different essential features, there are restrictions such as high-power utilization and dissipation, as well as leakage current, which are taking the development bend of the industry downwards. Silicon-based 3D density gradient nanowire MOSFET [8] has made its position more grounded than before with its high performance and cost-effective applications. However, the theoretical limitations of silicon-based semiconductors lead researchers to search for newer materials. Keeping in mind the future limitations of Silicon, investigation of other available materials is currently one of the most hyped research fields. Gallium Arsenide (GaAs) can be a promising material for the semiconductor world and will lead to more readily available small, high-frequency products.

Presently, power scaling, device lifetime, and the continuation of Moore's Law are some of the major concerns of researchers. Continuation in development requires productive and compelling arrangements. There comes the significance of nanotechnology, which utilizes the bottom-up approach to construct nanoscale semiconductor devices in an arrangement with the confinements. Moving towards the nanoscale again brings up concerns about quantum effects like quantum confinement and tunneling. Various methods like Drift-Diffusion (DD) [1], Monte Carlo (MC)[2], and Non-Equilibrium Green's Function (NEGF) [2] [6] techniques. Later techniques are quite expensive and require complex calculations. However, the calculation of quantum confinement can be included by simply adding the Density Gradient (DG) theory and the conventional Drift-Diffusion theory.

This paper contains the following works:

- Designed two 3D density gradient nanowire MOSFETs using Si and GaAs as semiconductor materials.
- Tabulation of DC Analysis (Id-Vg curve, Id-Vd curve, electron concentration along x and z coordinates) and AC analysis (gm-Id curve) of both the designed models.
- Extracted model files and library files of the designed models.
- Designed a simple inverter circuit using the MOSFETs model and library files to show a digital application of the designed models.
- Designed a self-biasing circuit to show the frequency response of the designed models.

The goal of the above-mentioned works is to provide an

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analytical comparison of the impact of Si and GaAs as semiconductor materials in designing 3D density gradient nanowire MOSFETs. The comparison is made from model design and analysis to application-level analysis.

II. Literature Review

Extensive research has been going on since the start of the semiconductor industry. Researchers have led the paths from using a limited number of transistors to making up to large-scale ones and presently in nanoscale version. M. G. Ancona provided a macroscopic approach to modeling quantum transport that is particularly adapted to semiconductor device analysis and engineering [1]. He commented that the approaches should depend on the nature of work and interest, and those can be complemented accordingly to get the required results [1]. S. Jin et al. presented and developed models and tools based on Drift-Diffusion (DD), Monte Carlo (MC), and Non-Equilibrium Green's Function (NEGF) techniques, which are encapsulated in the Glasgow 3D statistical 'atomistic' device simulator [2]. They showed the importance of selecting values of the fitting parameters like Density Gradient (DG) effective masses for getting exact results. S. C. Jain et al. have obtained a simple expression for BGN in n-GaAs, which agrees well with recent luminescence and transistor measurements [3]. The team found numerically fitted simple expressions to the impurity scattering part of a BGN obtained using the multiple scattering theory [3]. Jing Wang et al. did a computationally efficient three-dimensional quantum simulation of various silicon nanowire transistors based on the effective-mass approximation [4]. Yiming Li et al. computationally investigated the electrical characteristics of germanium (Ge) nanowire field effect transistors (FETs) [5]. They compared Ge with Si based on electrical characteristics through the model formulation and parameter extraction, which play a significant role in device application in the industry [5]. R. Brown et al. compared the density gradient approach with a mode-space non-equilibrium Green's function (NEGF) simulator before using it to simulate the random dopant-induced variability in nanowire MOSFETs [6]. They estimated that definite values of effective mass and a specific range of values of gate voltage could be made possible to match the threshold voltage shift and subthreshold slope of the simulated I-V characteristics, as well as the electron distribution [6]. S. Rhee et al. studied a method to reduce the difference between the simulation results of Density Gradient (DG) and Schrödinger–Poisson (SP) when analyzing the effect of discrete charges, such as random dopants and interface traps, in sub-10 nm MOSFET devices in terms of electrostatics [7]. The observation showed a random electron density variation at the center of discrete charge in the conventional DG simulation, even when the device's size has been reduced [7]. Awanit Sharma et al. explained the performance analysis of a Gate-All-around silicon nanowire with an 80nm diameter field effect transistor-based CMOS-based device utilizing the 45-nm technology [8]. Mohinder Bassi et al. applied high K dielectric material, which has better gate controllability, which made nanowires a more promising device for low-power applications [9]. Issues through failure modes, symptoms, and algorithms during designing to reduce the problems of SiC MOSFET applications were investigated and evaluated by B.J. Nel and S. Perinpanayagam [10]. A junction-less nanowire MOSFET has been investigated through FOMs for cryogenic temperatures and underlapped length variation by Sasank, T. Sai, et al. [11]. A core insulated double gate MOSFET has been designed for removing short channel effects, and characteristic parameters have been evaluated by Jaiswal, S., Gupta, S.K. [12].

This paper brings up the analytical and application-level comparison of the impact of Si and GaAs as semiconductor materials in designing 3D-density gradient nanowire MOSFET. The density gradient (DG) theory and the conventional drift-diffusion (DD) theory have been used to include quantum confinement in calculation while evaluating the characteristics of 3D density gradient nanowire MOSFETs. The designed models have been assessed through DC and AC analysis. Then, the evaluated data was used to generate model and library parameters. Through these parameters, the model has been used to design digital and biasing circuits to show the application-level comparison of the developed models.

III. Methodology

A. Density gradient theory:

The density gradient (DG) theory involves easy calculations, with few additional parameters to be added to the drift-diffusion (DD) model [13]. This helps to include the quantum confinement effects in required calculations in a cost-effective and less time-consuming way.

Drift-diffusion theory includes charge conservation laws. This theory has been used in classical physics for a long time due to its consistency and continuum involvement of required parameters for providing accurate results [13]. Semiconductor devices work either in a forward or reverse direction by the average flow of electrons and holes throughout the implicit structure of the device. This average flow of electrons and holes generates current flow in the opposite direction of the electron flow. The flow of current and electric charges created by the movement of charge is known as the drift-diffusion theory in simple words [13]. This theory includes charge, electric field, and energy states at its fermi level. All related equations are given in [1], [6], [13].

The continuous reduction process of the size of the semiconductor device leads to the classical models being unable to provide accurate results [1]. With a reduction in size, quantum effects no longer remain negligible. Among them, the most concerning ones are quantum confinement and quantum tunneling. This has brought up the need to amend the

classical models to quantum-included ones. Among many available expensive and complex models, the density gradient theory is the easiest to include with the classical model with the least addition of parameters and complexity. These need to add a few more parameters, including quantum confinement, with the classical drift-diffusion model. The mentioned theory adds quantum potential with the quasi-fermi levels, which further require effective mass as fitting parameters, recombination rates, and Slotboom variables [1], [13]. In addition, it needs to be included that the density gradient theory, along with the simple drift-diffusion model, includes quantum confinement only, and quantum tunneling is not included.

B. Material properties of GaAs and Si:

The material properties of GaAs and Si can be compared to get a theoretical analysis of the impact of two varied materials in designing the nanowire MOSFET. Table I contains the material properties of the two materials [14].

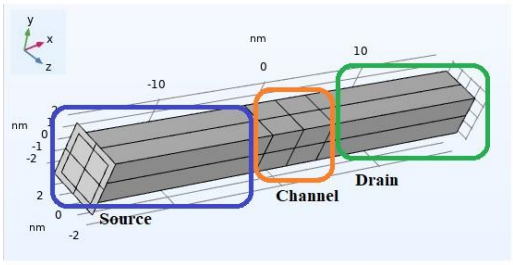
TABLE I. MATERIAL PROPERTIES OF GaAs AND Si.

Material Properties	**GaAs**	**Si**
Structure	Zinc Blende	Diamond Cubic
Band Gap Energy (eV)	1.42	1.12
Lattice Constant (Å)	5.653	5.431
Nature of bandgap	direct	indirect
Refractive index	3.3	3.42
Dielectric constant	12.9	11.7
Thermal conductivity ($W/cm^{-1} L^{-1}$)	0.46	1.56
Electron Mobility ($cm^2/V\text{-}s$)	8000	1400
Hole Mobility ($cm^2/V\text{-}s$)	400	500
Electron saturated velocity (10^7 cm/s)	0.7	2.3

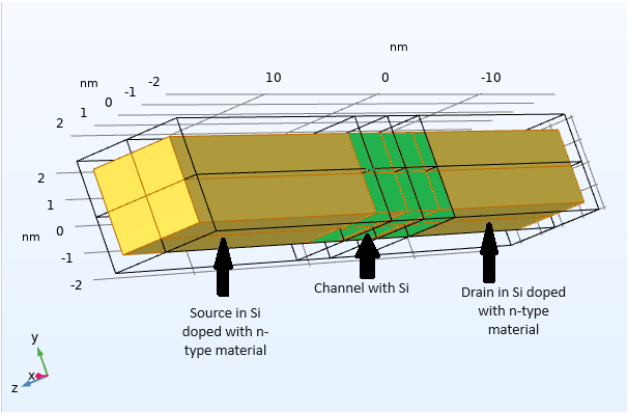
From the above table, it can be said that GaAs is theoretically a better material for designing a MOSFET as its Band gap energy, lattice constant, dielectric constant, and electron mobility are higher than Si's. However, Si's thermal conductivity and electron saturated velocity are lower than those of GaAs, which is also suitable for MOSFET design.

C. Model Description:

The model is designed so that the two sides have the source and drain. Rectangle-shaped structures have been built where the inner square has a width equal to 3.2nm, and the outer square has a width of 4.2nm. A channel is created in the middle to connect the two terminals. The middle part is the channel creating a path for current flow from the source to the drain. The channel is surrounded by gate oxide from all sides. The oxide layer covering the source, channel, and drain has a depth of 0.5nm. The whole model is surrounded by an oxide layer (SiO_2). Figure 1 shows the labeled source, channel, and drain of the 3D geometry of the designed nanowire MOSFET. The length of the source and the drain is 15nm each.



(a)



(b)

Fig1. 3D geometry of nanowire MOSFET (source, channel, and drain): (a) Labelled source, channel, and drain. (b)The yellow part shows the source and drain in Si-doped with n-type material, and the green part shows the channel in Si.

The channel, which has a width of 3.2 nm, is created in the middle between the source and the drain. It creates the path for the current flow in the semiconductor device. The whole model is surrounded by an oxide layer (Silicon Dioxide (SiO_2)) on top and has a gate all around on top of the channel in the middle. So, the designed model finally looks like the following figure 2.

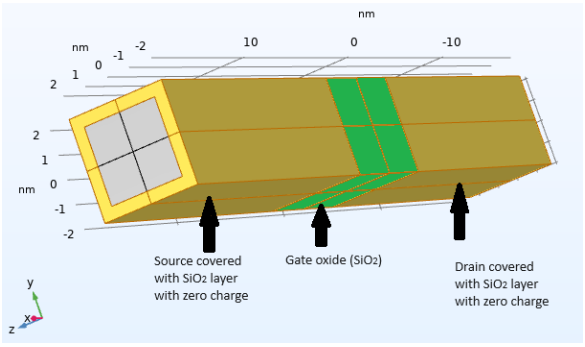


Fig2. 3D geometry of nanowire MOSFET (surrounded by SiO_2 and gate oxide in the middle surrounding the channel)

There is inconsistency in the effective mass throughout the 3D geometry in this model [3]. For this first, the effective mass along the longitudinal and transverse axes is set at 0.8 and 0.12, respectively [8]. For including a Density Gradient (DG) effect in the physics simulations, the effective mass is set diagonally for the x, y, and z axes. The analysis is based on a few values of the longitudinal DG effective mass (fmx=0.1, 0.2, 0.3, 0.5, 0.8). The oxide layer surrounds the source, drain, and channel on the outside using the Charge Conservation laws. The quantum confinement effect is considered when specifying the boundary conditions for the insulator interface. The addition of trap-assisted recombination to semiconductor physics is for small signal AC analysis. The harmonic perturbation and differential computation have been included with the drain metal contact and gate terminal to accurately assess the small-signal analysis.

D. MOSFET Model Application in Digital Circuit Design:

Characteristic curves like I_d-V_g, I_d-V_d, and the small signal analysis curve gm-Id have been extracted for the designed models. A model file has been generated utilizing values from the extracted curves. This model file requires values from gm-I_d, I_d-V_{ds}, and I_d-V_{gs} which are extracted from the curves and values of C_{gd}, C_{gs}, C_{ds} R_{ds} (drain-source resistance), R_d (drain resistance), R_g (Gate resistance) taken from [15], [16]. The formulas to calculate the Kp, Ciss (input capacitance), Coss (output capacitance), and Crss (reverse transfer capacitance) were taken from [17]. A library file has been generated from the model files for the designed NMOS nanowire MOSFETS. Using the created NMOS models, a digital inverter circuit has been finally designed, and output is observed. Finally, the frequency response curve for both models has been generated using a biasing circuit. This provides an application-level comparison between the two designed 3D-density nanowire MOSFETs with semiconductor materials such as Si and GaAs. The model library file generation and circuit design have been done utilizing the extracted data from the analysis curves. Table II below shows the parameter values defined in the generated library file for the models used by Si and GaAs, respectively.

TABLE II LIBRARY PARAMETERS OF Si and GaAs USED NANOWIRE MOSFET MODELS

Parameter Name	Value for Si used model	Value for GaAs used model
CBD (F)	1.986e-19	30e--15
CGSO (fF)	0.006	32
CGDO (fF)	0.001	398
Kp (GAV^2)	91.26	100.62
L (nm)	3.2	3.2
RD (mohm)	3.38	1.5
RG (ohm)	11.76	1.4
RDS (Mega ohm)	1	2
TOX (nm)	0.5	0.5
VTO (V)	0.7	0.7
W (nm)	3.2	3.2

IV RESULT AND DISCUSSION

The DC and AC analysis of the designed models was done, and the results can be tabulated in Table III [18].

TABLE III RESULTS FROM DC AND AC ANALYSIS OF THE DESIGNED Si and GaAs USED NANOWIRE MOSFET MODELS

	Si	GaAs
I (A)	20×10^{-6} (fmx=0.8)	14×10^{-5} (fmx=0.8)
	33×10^{-6} (fmx=0.1)	18×10^{-5} (fmx=0.1)
VT (V)	0.7	0.7
Vd (V)	0.5	0.5
Electron Concentration along x-coordinates ($1/cm^3$)	10^{16} - 10^{20}	10^{12} - 10^{20}
Electron Concentration along z-coordinates ($1/cm^3$)	10^{15} - 10^{17}	10^{11} - 10^{15}
gm (uS)	(10^{-4} - 10^{1})	(10^{-8} - 10^{4})

It is apparent from the table that the material GaAs has a higher drain current at a similar threshold voltage than the Si-used model. The threshold voltage for both models is 0.7V. The drain current for the GaAs-used model is approximately ten times greater than the Si-used model. This is suitable for analog circuit design. Though some switching losses might be faced, that will be minimal if kept within the safe operating area. Again, the GaAs-used model has a drain current of higher value by ten times that of the Si-used model. It is evident from the table above that the potential well depth formed by the model using GaAs as a material is much deeper than the model with Si for both the x and z coordinates. From the table, it can be evaluated that the resultant value of the transconductance is much higher in the case of the made model than the Si model.

The values extracted from the above table, along with the capacitances and the resistances values, have been taken to generate model and library files. The NMOS component created using the files for both Si and GaAs models was used to create a simple inverter and biasing circuits to show the application-level comparison of both models. The simple inverter circuit and the biasing circuit are shown in Figures 3 and 4, respectively.

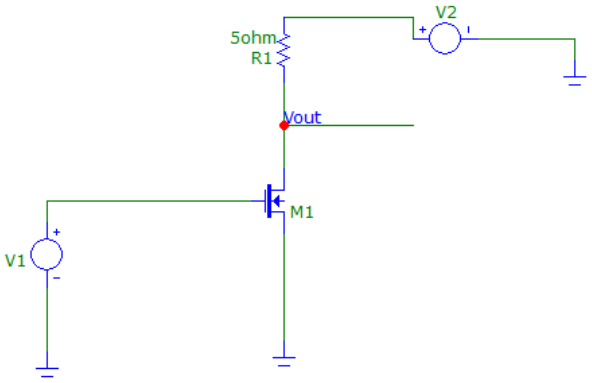


Fig.3. Circuit Diagram of simple inverter circuit.

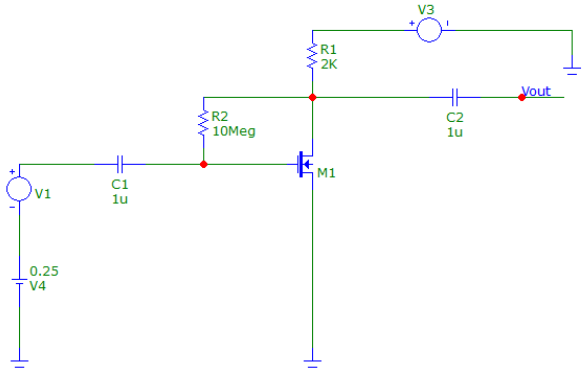


Fig. 4. Self-biasing circuit for frequency response analysis.

The inverter circuit shows accurate results, providing 0V at the output when input is given as 1V and vice-versa. Figure 5 shows the output of the inverter circuit for both models.

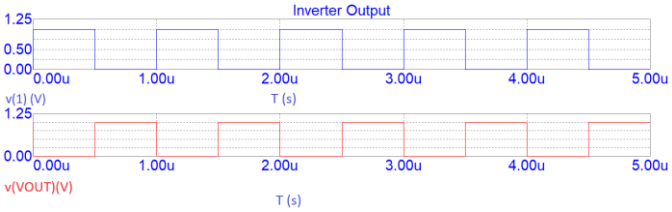
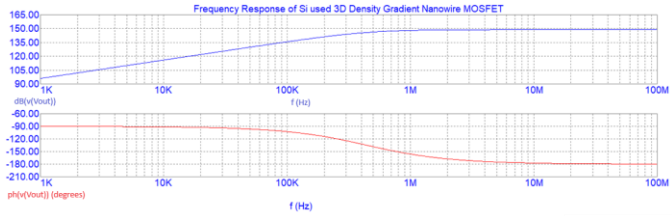
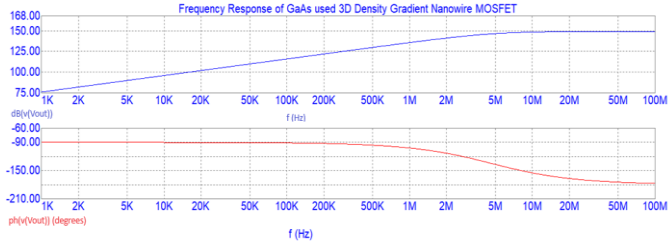


Fig. 5. Inverter circuit output of both Si and GaAs used models.

Lastly, the frequency response curve in dB and phase change curve have been generated for both models. The results are shown in Figures 6 (a) and (b).



(a)



(b)

Fig.6. (a) Frequency response curve of Si used model. (b) Frequency response curve of GaAs used model.

From Figure 6 (a) and (b), the used model has a cut-off frequency at 1MegaHz while that of the GaAs used model is at 10MegaHz.

Si has been there since the start as a major material in the semiconductor industry. However, with the reduction in the size of the devices, few limitations are coming up and researchers are going for newer materials to take the place of Si. From the analytical results, it can be said that GaAs can be a better material, impacting the performance and features of devices in the semiconductor industry.

V Comparison with Previous Works

A comparison table has been shown for differentiating the designed model from available research papers. The comparing parameters have been limited to the channel length, oxide thickness, and threshold voltage.

TABLE IV. COMPARISON WITH PREVIOUS WORKS

Research Works	Channel Length[nm]	Oxide Thickness [nm]	Threshold Voltage [V]
[19]	30000	7	0.125
[20]	10	3-10	0.2
[21]	7-10	2.82	0.7
[6]	4	0.8	0.7
Designed Model	3.2	0.5	0.7

Table IV shows that the value of threshold voltage increases with the decrement of channel length and oxide thickness. Moreover, the designed model has the lowest values of channel length and oxide thickness among the mentioned papers.

VI CONCLUSION

The paper analyzes the impact of semiconductor materials in designing the 3D density gradient nanowire MOSFET. The models having the same channel length and oxide thickness of 3.2nm and 0.5nm, respectively, have been designed using varied materials, namely Si and GaAs. I_d-V_g, I_d-V_d, gm-Id curves, and the electron concentration along the x and z coordinates have been analyzed and compared. The analysis showed the drain current, potential-well depth, and transconductance values are higher by approximately 10, 10^4, and almost double in range, respectively, in the case of the

model designed using GaAs as a material compared to the Si-used model. The higher drain current can provide switching losses, which can be controlled if kept within a safe operating area. In addition, a higher drain current is suitable for application in analog circuit designs like amplifiers. Moreover, the extracted data have been utilized to generate model and library files to create a component model. A simple inverter circuit and biasing circuit have been designed with the models to get a digital application-level comparison. The inverter circuit worked accordingly, and the frequency response curve provided the cut-off frequency of both models. It is found that the Si-used model has a cutoff frequency of 1MHz while that of the GaAs-used model is 10MHz, which means the used model can provide faster performance. So, it can be said that the GaAs used model can offer faster performance and more energy than the Si one. From the theoretical and analytical comparison from analysis to application level, it can be concluded that the model using GaAs as the material would give better and faster performance than the model using Si material. Further work might include designing low-power analog application circuits to get analog application-level analysis of the designed nanowire MOSFET.

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