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Design, simulation and optimization of a single stage Low Noise Amplifier (LNA) for very low power L-Band satellite handheld applications.

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Abstract- In first stage of each microwave receiver, there is a Low Noise Amplifier (LNA) stage, and this LNA plays an important role to determine the quality factor of the receiver. The design of a LNA requires the trade-off of many important parameters including gain, Noise Figure (NF), stability, power consumption, cost and design complexity. In this paper, we have designed and simulate a single stage stable LNA circuit having gain 11.78 dB and noise figure 1.86 dB using microwave BJT AT3103 **with Agilent package Advance Design Systems (ADS). This LNA operates at center frequency of 2 GHZ and it can be used in L-Band satellite modem for tracking applications.**

Key words: Low Noise Amplifier, Radio Frequency, Advance Design System, Noise Figure, single stage, multiple stage

I. Introduction

Demand for both satellite and wireless communication system with higher data rate is tremendous and this demand is exponentially increasing with increased consumer demand [1]. Low-noise amplifiers (LNA) are the building blocks of any wireless communication system. LNA is usually located very close to the receiving antenna to amplify captured weak signal [2]. The design challenge in LNA is to achieve low noise figure (NF) and high gain simultaneously while maintaining low power consumption [3]. A properly designed LNA with high gain will reduce overall noise from subsequent stages of receiver tremendously as shown in equation (5) and (6). However, the inherent noise of LNA itself is injected directly into the system and impact sensitivity negatively [2]. LNA is one of the most power-hungry and area consuming component in wireless receivers [2]. A single stage LNA could rarely meet high gain requirements, however single stage is the least power consuming topology [4], [5].

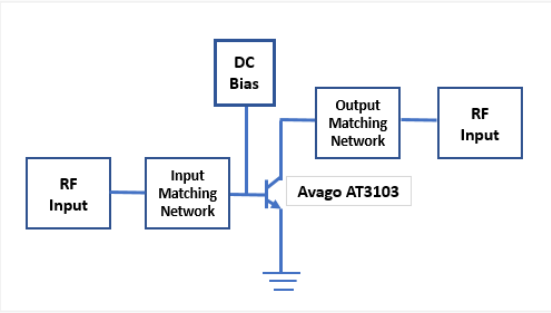

Fig. 1: General Structure of a LNA in Block Diagram.

In this paper, we designed a low power, moderate gain, matched and stable LNA for L-band applications. This paper is organized as follows: Section II discusses on LNA design parameters. In section III, we summarise our design and optimization process. Section IV, presents the optimised simulation result. Section V and VI, concludes the paper with acknowledgement and conclusion.

II. DC biasing and Design parameters

The selected transistor for this low power LNA is an NPN bipolar junction transistor numbered AT3103 and it is fabricated by Avago Technologies. Typical application of this AT3103 is in cellular, PCS handsets as well as Industrial-Scientific-Medical systems. To design a low noise amplifier, we must have to bias the transistor at an operating point that suits our design requirements [2]. The bias point can be selected either for low noise or high gain or high power or low power etc [6]. Biasing network is also responsible for mismatch in source side and load side of LNA. A low and allowable VSWR at input side and output side confirms that matching is proper and the LNA is stable. We can see in Fig.1, a simplified general structure of a LNA. Fig. 2 shows the biasing network of our optimized design, where we can see that LNA is drawing 1.63 mA of current from DC bias source.

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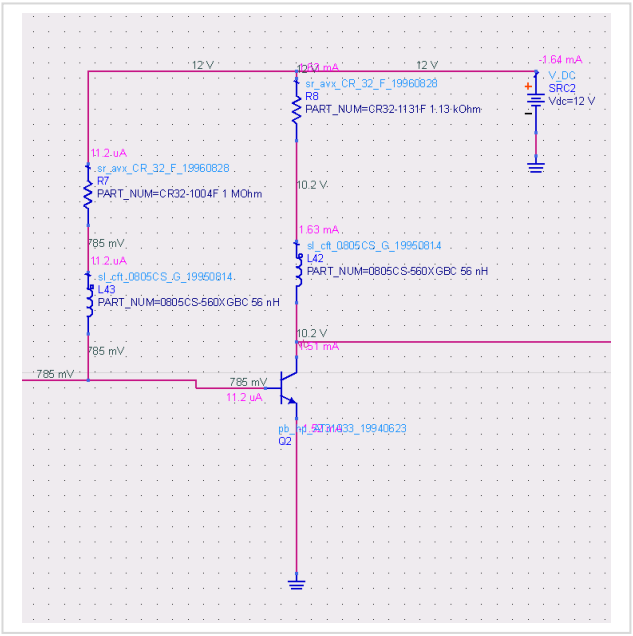


Fig. 2: Biasing of the designed single stage LNA with DC annotation in ADS.

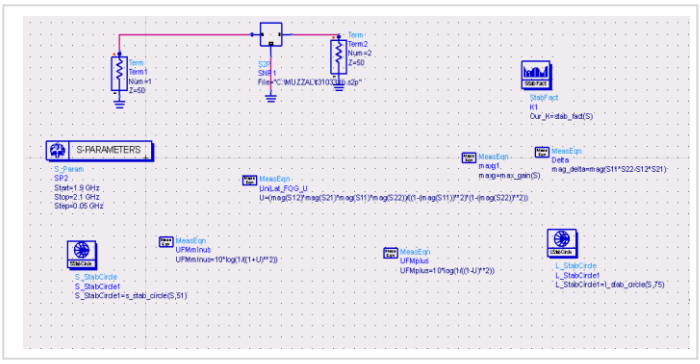


Fig. 3: A sample simulation setup employing S2P of AT3103 in ADS.

After biasing the BJT transistor for our desired low power and minimum noise requirements, we had shifted our focus to the optimisation of other design parameters. The S2P file of the AT3103 have all the RF information for different frequency to simulate the performance of our LNA. A sample S2P based simulation in ADS to check the stability of our design is shown in Fig. 3.

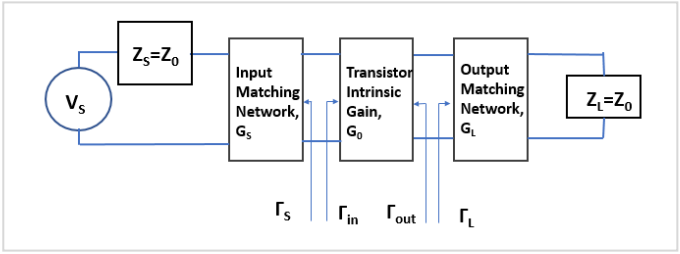
Stability, in amplifiers, refers to an amplifier's immunity to have spurious oscillations arising from unwanted positive feedback [7]. If we can ensure S_{12} to a very low level, we can assume the system to be unilateral. Any network can oscillate if it sees real impedance which is negative in value. Rollett's stability factor is another way to decide whether a system is stable or not through measuring K-factor and |Δ| as shown in equation (1) and (2). Value of Voltage standing wave ratio (VSWR) from input side and output side of LNA also confirms us on amount of reflection and hence the stability of the system.

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{11}S_{22}|} \quad (1)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (2)$$

For unconditional stability of a LNA, K>1 and |Δ|<1.

VSWR is a measure of how efficiently radio-frequency power is transmitted from a power source, through a transmission line, into a load. This requires an exact match between the source impedance, the characteristic impedance of the transmission line and all its connectors, and the load's impedance. VSWR on a transmission line is mathematically related to the ratio of reflected power to forward power. If the impedance of the load is not identical to the impedance of the transmission line, the load does not absorb all the RF power and reflection happens. This reflection creates a pattern of voltage peak and voltage valley on the transmission line. VSWR is the ratio of the highest voltage value anywhere along the transmission line to the lowest voltage value [7]. In an ideal system with no reflection VSWR=1.0. When reflections occur VSWR becomes higher.



$$VSWR = |V_{max}| / |V_{min}| \quad (3)$$

where V_{max} is the maximum voltage of the signal along the line, and V_{min} is the minimum voltage along the line.

The maximum power-transfer theorem says that to transfer the maximum amount of power from a source to a load, the load impedance should match the source impedance. If the impedances aren't matched, maximum power will not be delivered. In addition, standing waves will develop along the line. The impedance matching device may be a component, circuit, or piece of equipment. A block representation of a LNA with matching network and arising reflection co-efficient is shown in Fig. 4. Noise factor, F is a measure of how the signal to noise ratio is degraded by a device. It determines the efficiency, sensitivity and suitability of a LNA for low noise applications. F can be measured from SNR, as shown in equation (4).

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$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{\frac{S_{in}}{N_{in}}}{\frac{S_{out}}{N_{out}}} \quad (4)$$

For a receiver that composed of number of stages, each with its own noise figure and gain - noise factor can be determined with a formula developed by Friis as shown in equation (5).

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_N - 1}{G_1 ... G_{N-1}} \quad (5)$$

which can be simplified for a receiver, having a LNA in the first stage to be:

$$F_{total} = F_{LNA} + \frac{F_{rest} - 1}{G_{LNA}} \quad (6)$$

where F_{rest} is the overall noise factor of the subsequent stages of a receiver. According to this equation, the LNA can reduce the overall noise figure of the receiver, if it has high gain.

Fig. 4: Block representation of a Single Stage Low Noise Amplifier with input and output matching network.

Noise figure, NF is the noise factor, expressed in decibels.

$$NF = 10\log(F) = 10\log(\frac{SNR_{in}}{SNR_{out}}) = SNR_{in,dB} - SNR_{out,dB} \quad (7)$$

Minimum detectable signal (MDS) in a receiver is the smallest input signal power, equal to noise floor of system, that can be processed by its conversion chain and demodulated by the receiver to generate usable information at output. Generally, the lower the noise figure, the lower is the receiver MDS and the more sensitive the receiver is.

The LNA shown in Fig. 4, having source, Z_s and load impedance, Z_L models the mismatch at input and output. The overall gain for this LNA can be given by:

$$G_T = G_S G_O G_L \quad (8)$$

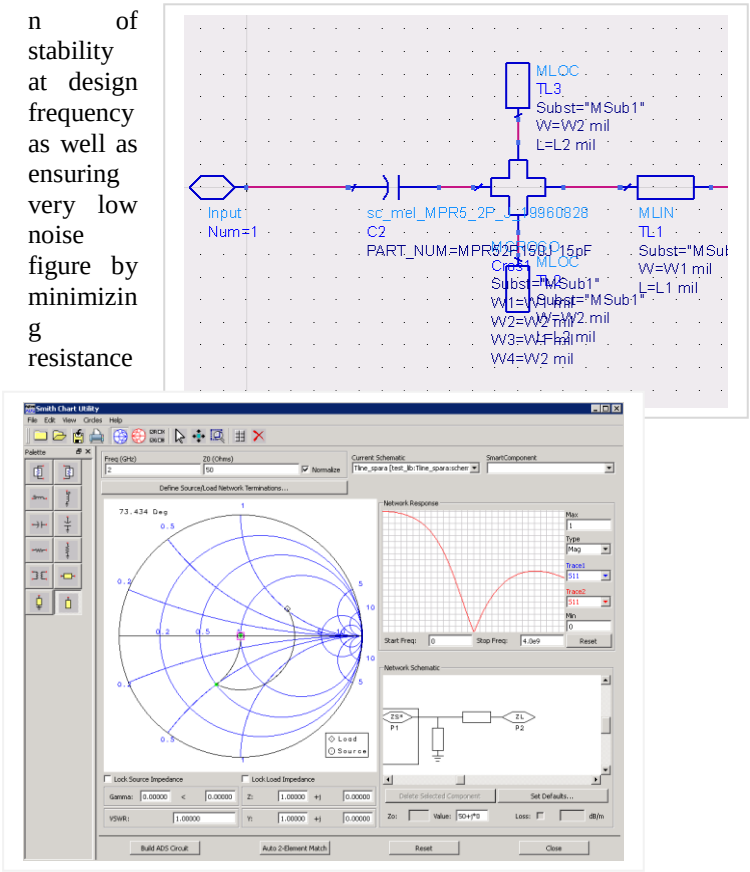
where, G_S and G_L are effective gains due to the impedance matching of the transistor at input and output.

III. Design and Optimization process

An appropriate bias circuit is the first step in the design of a LNA. In our design, we had chosen a common emitter configuration for AT3103. Isolation between RF and DC part of the circuit was achieved by using the RF choke and condensers. In the second step, we synthetize input and output reflection coefficients to ensure the stability, low noise figure and high gain. For matching purpose, a solution with open stubs was used, both at the input and the output of LNA. Last step was the fine tuning and optimization of the lengths of the transmission lines in the matching circuit to minimize the noise figure of the amplifier and maximize the gain. It was done by applying several optimization algorithms until optimal solution and specifications are meet.

Some key steps in the design of our LNA are –

1. Selection of S-parameter model of the active device.
2. Inclusion of bias network that is required for the specified S-parameter of interest.
3. Evaluation of stability at design frequency as well as ensuring very low noise figure by minimizing resistance



use.

4. Plot of available gain (GA) and noise figure circles, from there we decide the design tradeoff between gain and noise.
5. Design of matching network for allowable VSWR value and plot the VSWR circle.
6. Simulate the design over wide frequency range and ensure that the design is stable over the range.

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7. Modify circuit if necessary with frequency-dependent stabilizing circuits.

Fig 5: Input matching simulation in ADS (short stub).
Fig 6: Output matching simulation in ADS (open stub).

IV. Simulation result and Optimization

In this section, we are reporting the simulation process, simulation result and the optimization process of our design. In Fig. 5 and Fig. 6, we can see the matching simulation setup in ADS at input and output of our LNA. Whereas, Fig. 7 and Fig. 8 shows the matching network of our optimized circuit at input side and output side.

Fig.7: Input Matching network.

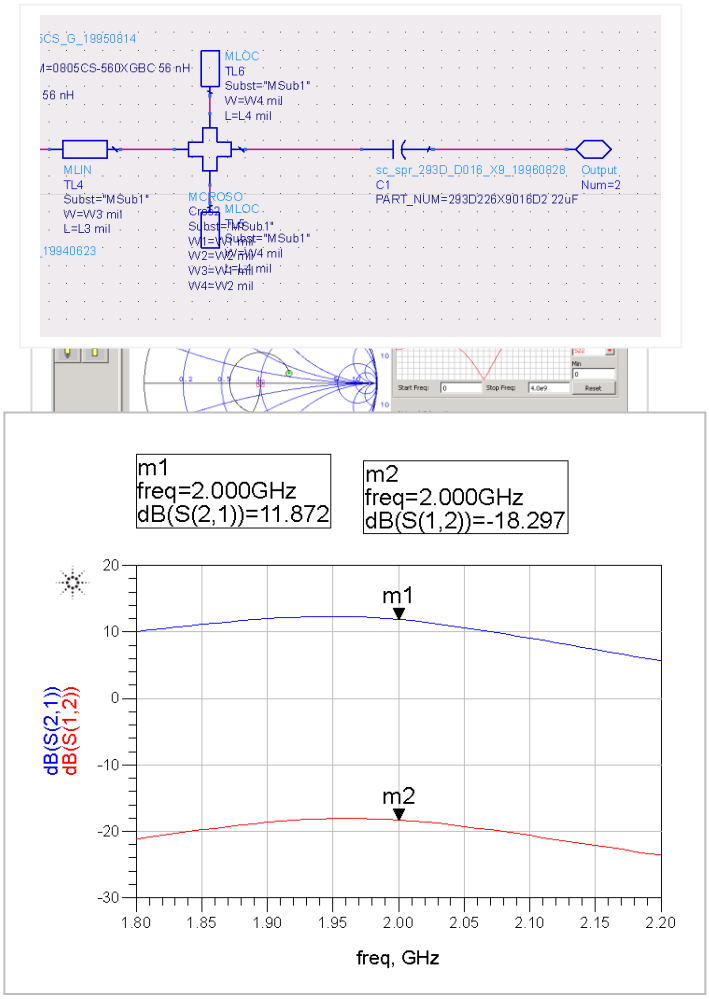
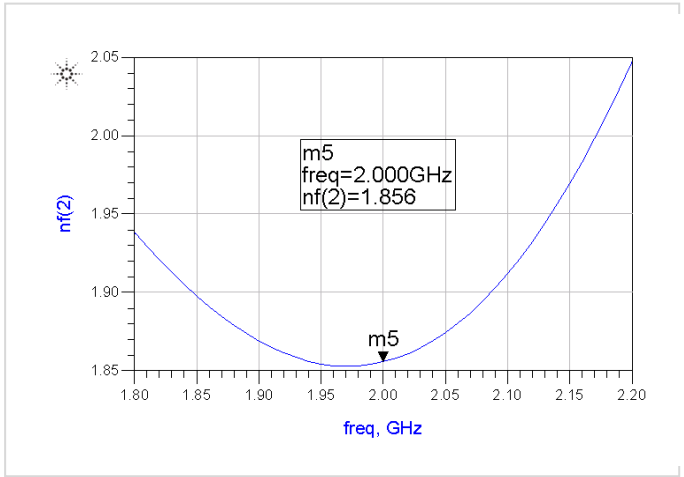


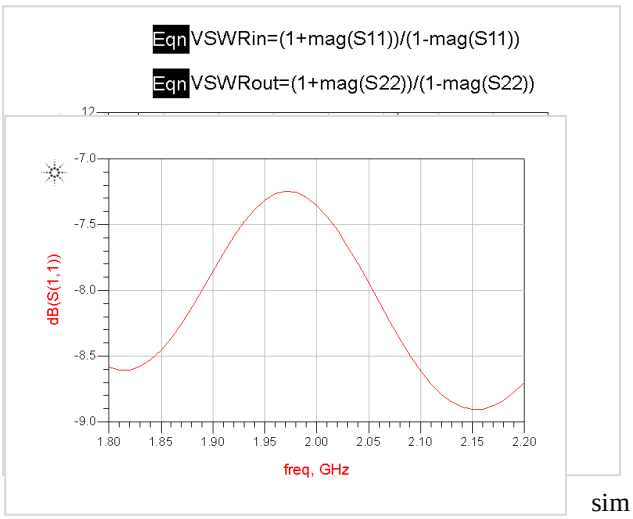
Fig.8: Output Matching network.
Fig. 9: Forward gain and Reverse gain of the LNA.



We can see from Fig. 9, that the forward gain and reverse gain of the optimized LNA to be 11.87 dB and -18.29 dB, respectively. Although in linear scale the forward gain from LNA is nearly 4, and it is enough for the subsequent stages to detect and amplify as required.

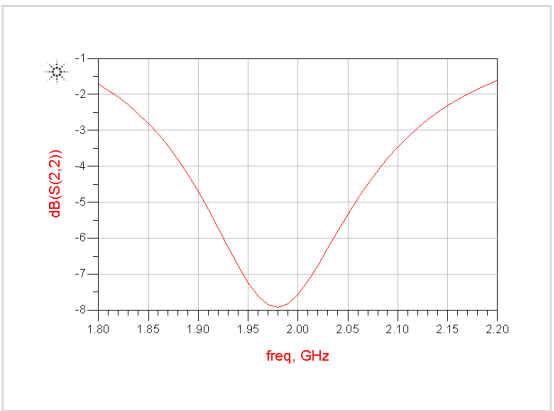
Fig. 10: Noise Figure of the designed LNA.
Fig. 11: VSWR of the optimized LNA.

We have checked the reflection co-efficient of our design by simulating VSWR from input side and output side as shown in Fig. 11. The input VSWR 2.5 and the output VSWR is 2.44, which are acceptable and within design specification for any standard LNA. We can also see the signal reflection



simulation of the LNA from input and output in Fig. 12 and Fig. 13. From there, we find that a very small value of -8dB of S_{11} and S_{22} ensures maximum power transfer with minimum reflection.

Fig. 12: Input Reflection Simulation of LNA.



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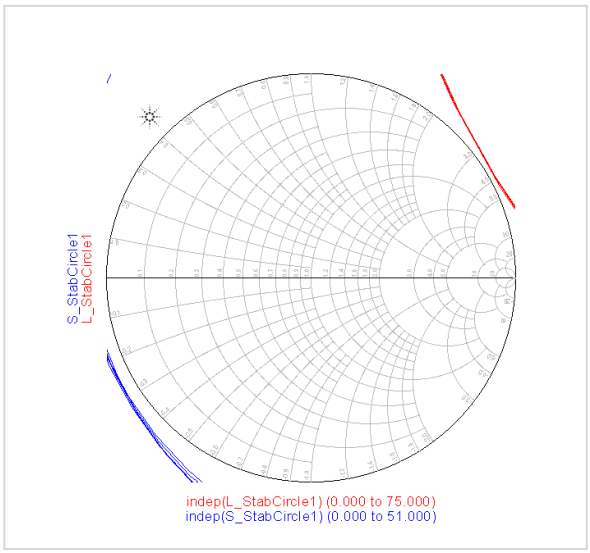


Fig. 13: Output reflection Simulation of LNA.
Fig. 14: Stability confirmation of optimized LNA in ADS.

We finally verified the stability of operation of our designed LNA by simulating the stability circle from source side and load side, as shown in Fig. 14. This simulation confirms operational stability of the LNA throughout its operational range as there is no intersection of stability lines with the Smith chart.

Fig. 15: Delta factor simulation confirms stability.

Fig. 16: K factor simulation of the designed LNA System.

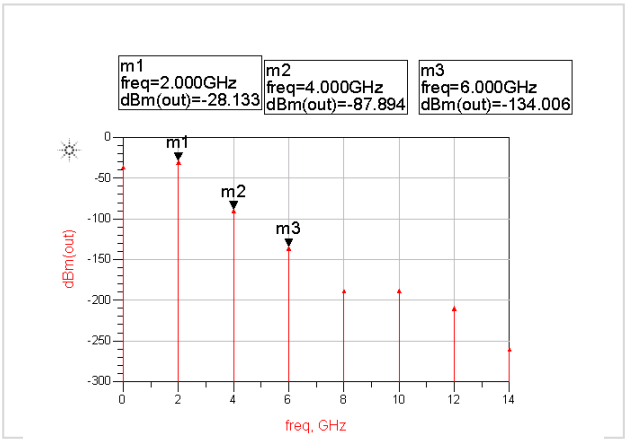
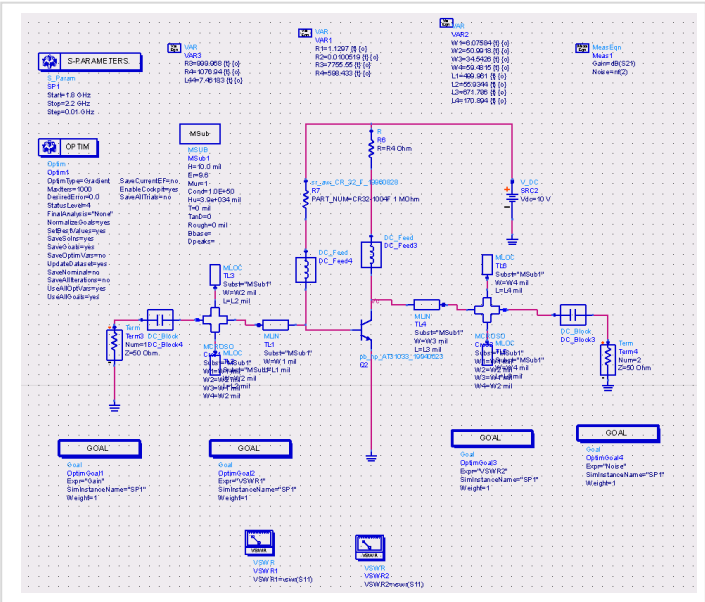


Fig. 17: Harmonic Balance Simulation at output of optimized LNA confirms domination of fundamental harmonics at 2GHz.
Fig. 18: Complete LNA with Matching and Bias network in ADS.

The value of Rollett's factor also confirms the unconditional stability of the Optimized LNA as shown in Fig. 15 and Fig. 16. We had stated in equation (1) and (2) that by ensuring k>1 and Δ<1, we can unconditional stability from our designed LNA.



We had also checked our design through harmonic balance simulation and found that fundamental component of input frequency is the most dominant component at the output of the designed LNA. The harmonic balance simulation is shown in

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Fig. 17. Fig. 18 shows the final optimized design of the LNA, where we can see the input matching network, output matching network and associated DC bias network. Finally, we layout the optimized design of the complete LNA for PCB fabrication as shown in Fig. 19.

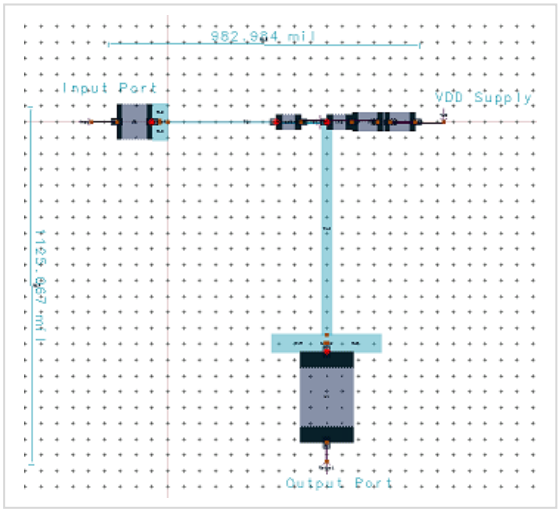

Fig. 19: Layout of the Optimized LNA with matching network.

V. Acknowledgement

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Table 1: Performance Parameter of the Optimized LNA

Parameter	Design Specifications	Achieved Value
Frequency	2 GHz	2 GHz
S21	>=11 dB	11.872 dB
VSWR (input)	<=3	2.501
VSWR (output)	<=3	2.44
Noise Figure	<=2dB	1.856 dB
S12	Not specified	-18.297dB
S11	Not specified	-7.3 dB
S22	Not specified	-8 dB

VI. Conclusion

A very low power BJT based low noise amplifier (LNA) has been designed and laid-out in Agilent Technologies simulation package ADS using Avago Technologies microwave transistor AT3103. The BJT transistor is biased to operate in Common Emitter configuration. This single stage, low power LNA is suitable for L-Band satellite application with operating frequency of 2GHz. It has a forward gain of 11.87 dB, noise figure of 1.86 dB, reverse gain of -18-3 dB as summarized in Table 1. To ensure low power consumption and to have better mobility operating time, we had biased this LNA with bias current of 1.64mA. The chip area estimate of the LNA from the layout is 7.1347 cm^2 which is equivalent to 983 mil × 1125 mil.

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