Published in AJSE, Vol:18, Issue: 02
Received on 27th June 2019
Revised on 23th August 2019
Accepted on 30th August 2019

AIUB JOURNAL OF SCIENCE AND ENGINEERING
ISSN: 1608 – 3679 (print) 2520 – 4890 (Online)

Gate Length Effect on Gallium Nitride Based Double Gate Metal-Oxide-Semiconductor Field-Effect Transistor

Md Rabiul Islam, Md Kamrul hasan, Md Abdul Mannan, M. Tanseer Ali, Md Rokib Hasan

***Abstract*— We have investigated the performance of Gallium Nitride (GaN) based Double-Gate (DG) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). Atlas Device Simulation Framework -Silvaco has been used to access Non-Equilibrium Green Function to distinguish the transfer characteristics curve, ON state current (I_{ON}), OFF-state current (I_{OFF}), Drain Induced Barrier Lowering (DIBL), Subthreshold Swing, Electron Current Density, Conduction Band Energy and Electric Field. The concept of Solid state device physics on the effect of gate length studied for the next generation logic applications. GaN-based DG MOSFETs shows better performance than Si-based Single gate MOSFETs. The proposed device has drawn the attention over conventional SG-MOSFET due to fas switching performance. The device turn on and turn off voltage is respectively VGS=1V(On state) and VGS-0V(OFF State). To validate our simulation tool and model results, previous research model has been investigated using Silvaco Atlas and the results obtained are compared to the previous results.**

***Keywords*— GaN; DG-MOSFET; DIBL, SS, Silvaco Atlas, SCE, Gate Length**

I. INTRODUCTION

The scaling with better enhancement in the device execution is the most fundamental objective of the microelectronics section. In such manner, the different device designing plans, for example, source/drain designing [1-2], double material-gate (DMG) innovation [3], channel designing [4-6] have been engaged from past decades One of the crucial parts of gate length engineering is to reduce Short channel effects (SCEs) adopting the concept on device scaling of Moore's law [7] contributing to the successive downscaling of MOSFETs is the most dynamic and prominent proclamation ensuring cost-effective smaller in size, high performance, low power consumption and switching speed [8].

Therefore, contracting the channel length causes losing control in the channel by a gate. As a result leakage current point out as short channel effects (SCEs) due to the channel short for losing control and acts as a capacitance. SCE ensues due to the consequence of the junction as the portion of channel desertion gate control [9]. The continuity of shrinking of gate length is performed for DG-MOSFETs owing to double gate both gate can control the channel region better and represents excellent electrostatic behaviour leads to reduce short channel effects [10].

However, to overcome this issue the channel demands multiple gates to control the area of the channel. However, a double gate (DG) metal oxide semiconductor field effect transistor (MOSFET) is the successor that has multiple gates to control the area of the channel precisely. DG MOSFET is referred to as auspicious applicant for better on state current and amnesty short channel effect (SCE) [11-15].

As conventional channel material has some major drawbacks, another channel material is needed for better performance for high switching activity. Charge carrier's excursion at a higher momentum than silicon by introducing the new channel material. Gallium Nitride (GaN) is the most preferable candidate as channel material with high power density, high thermal stability, and robustness because of its less effective mass and mobility is inversely proportional to the carrier effective mass. Channel material with HfO2 for GaN-based DG MOSFET is the outstanding contestant due to their endearing latent monument [16-18].

The channel length of GaN-based DG MOSFET is enhanced in both source and drain which causes to escalation effective channel length to overcome the SCE effect. However, the gate length is the most symbolic specification for better subthreshold slope (SS) and DIBL for GaN-based DG MOSFET [19-20]. Perhaps, compared to single gate conventional MOSFET, DG MOSFET if referred to as the most pledging applicant [21-22].

Md Rabiul Islam
American International University-Bangladesh
E-mail: saynova@hotmail.com

Md Kamrul Hasan
American International University-Bangladesh

Md Abdul Mannan
American International University-Bangladesh

M. Tanseer Ali
American International University-Bangladesh

Md Rokib Hasan
American International University-Bangladesh

II. PROPOSED DEVICE STRUCTURE

The proposed GaN-based DG-MOSFETs was investigated for multiple gate length using Silvaco Atlas. The length from source (n-channel) to drain (n-channel) is 5nm. The gate-1 and gate-2 have high-k hafnium dioxide (HfO_2).

In the proposed device, n-channel doping is doped at 10^{-20} cm^{-3} and p-channel doping is doped at 10^{-17} cm^{-3}. The equivalent oxide thickness and the gate work function is 0.59 nm and 4.48 eV. The proposed device model has been shown below,

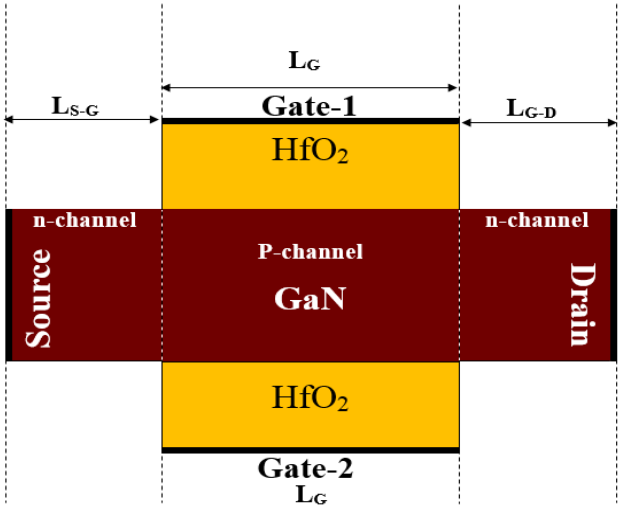

Figure1: Proposed Model of GaN-based DG-MOSFET

TABLE 1: SEMICONDUCTOR OVERVIEW

Description	Silicon	Gallium Nitride
Electron mobility (cm2/V-sec)	1450	2000
Critical field, 106 (EC)(V/cm)	0.25	3.0
Band gap (EG) (eV)	1.1	3.2

The above table demonstrates the difference between the two-semiconductor silicon (Si) and Gallium Nitride (GaN) according to International Technology Roadmap for Semiconductors (ITRS).

TABLE 2: SCALING PARAMETERS

Parameter Name	Description	Value
L_G	Gate length	9.1nm
E_{OT}	Oxide thickness	0.59nm
me*	Mass of GaN	$0.18m_0$
V_{DS} (V)	Drain Voltage	0.75V
V_{GS} (V)	Gate Voltage	1V

Table 2, describes the parameter used in simulation using Silvaco Atlas.

III. RESULT ANALYSIS

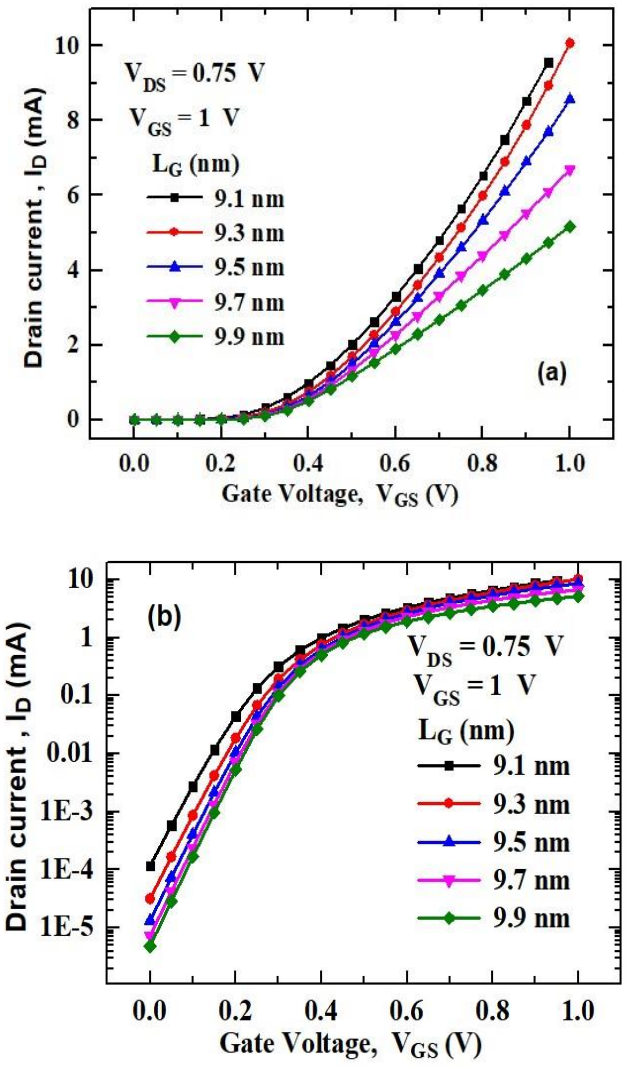

Figure 2: Transfer characteristics curve

The above figure represents the transfer characteristics curve, Drain current I_D vs. Gate voltage V_{GS} for the gate length of 9.1nm (a) Linear scale observation and (b) Log scale observation. The transfer characteristics curve for above-mentioned gate length of GaN-based DG MOSFETs, while considering at constant drain voltage, VDS = 0.75 Volts and voltage of gate, VGS = 1 Volts and equivalent oxide

thickness, EOT=.59 nm. From figure 1, it has been shown that by reducing the gate length higher current can drive.

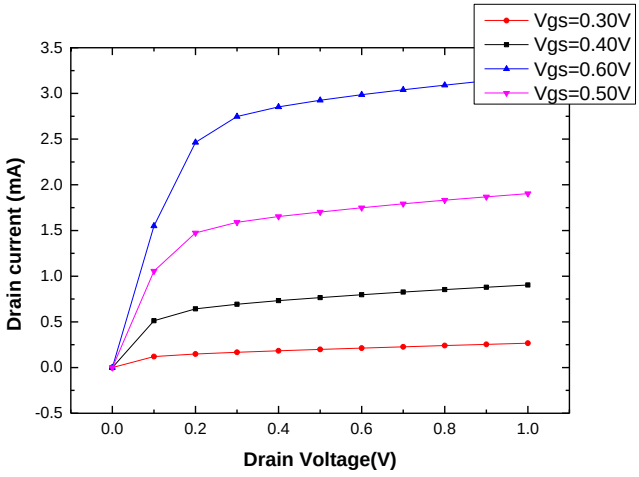

Figure 3: Output characteristics curve

The above figure shows the DC output characteristics curve for the proposed device of GaN based DG MOSFET for the gate length of 9.1nm.

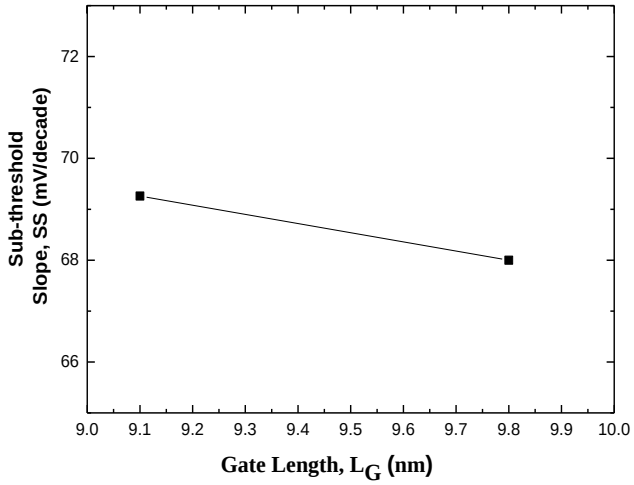

Figure 4: The effect of subthreshold slope

Figure 4, represents Sub-threshold swing for the gate length of 9.1 nm and 9.8nm. represents the change in SS against gate length and according to ITRS, the value is very convenient. The sub-threshold slope is measured as 69.3mv/decade and 67.9mv/decade for the gate length of 9.1nm and 9.8nm respectively. Sub-threshold slope is decreasing with respect to increasing the gate length.

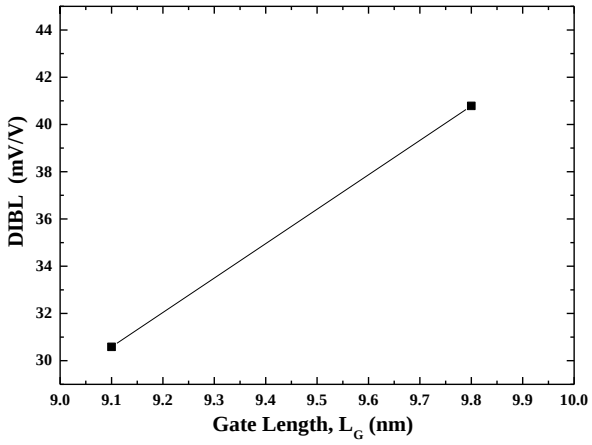

Figure 5: The Effect DIBL with respect to the gate length

The above figure represents the gate length effect on DIBL for the gate length of 9.1nm and 9.8nm. The critical electrical parameters such as DIBL is the difference of Vth owing to the difference in V_{DS} defined the electrostatic function of MOSFET [23]. DIBL is decreasing with increasing the gate length. DIBL is measured 31mv/V and 41mv/V for the gate length of 9.1nm and 9.8nm respectively. DIBL is decreasing with increasing the gate length.

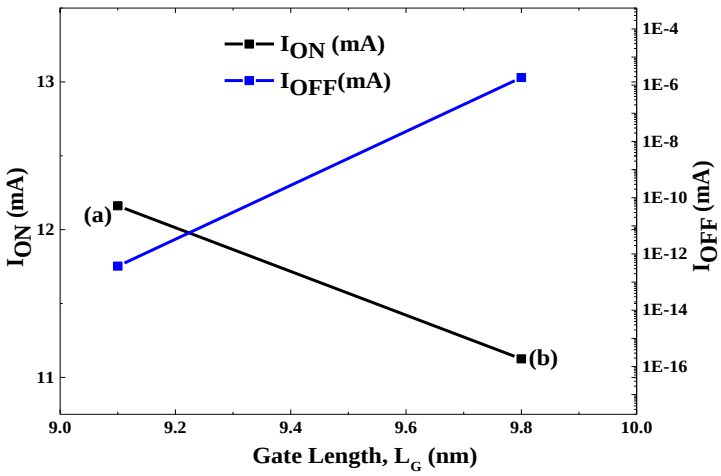

Figure 6: ON-state and OFF-state current with respect to gate length.

The above figure represents On state and OFF state current for the gate length of 9.1nm and 9.8nm. On state current is found 12.1 mA/μm and 11.2 mA/μm respectively. On state current is increasing with respect to decreasing the gate length. OFF state current is found $1E^{-12}$ mA/μm and $1E^{-6}$ mA /μm for the gate length of 9.1nm and 9.8nm. OFF state current is increasing with respect to increasing the gate length.

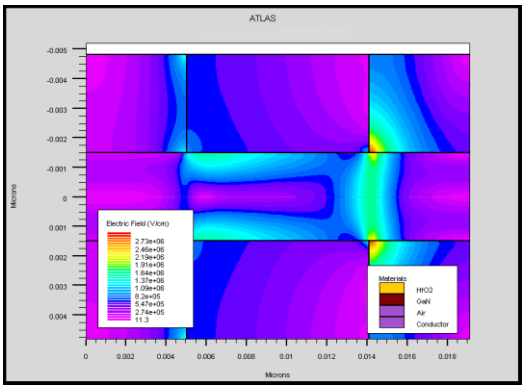

Figure 7: Electric Field for ON state current

The above figure represents the electric field for on-state current of GaN-based DG MOSFETs. All the material are identical with separate color. Figure 5, shows the impact of the electric field, E (V/cm) location toward the channel, x (nm) has been investigated since the voltage of drain, VDS=0.75 V, the voltage of gate, VGS= 1 V, EOT= .59 nm was considered for the gate length of 9.1nm.

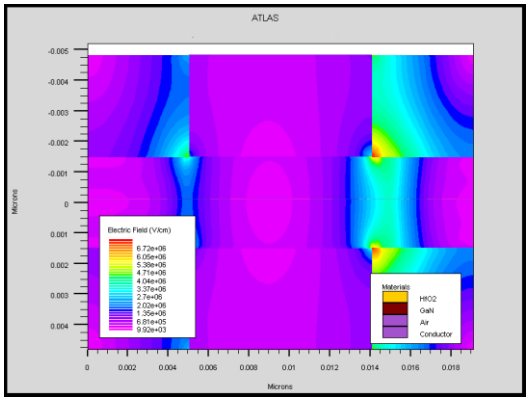

Figure 8: Electric field for OFF-state current

Figure 8 shows the electric field for OFF-state current for the gate length of 9.1nm with E_{OT} = 0.59nm.

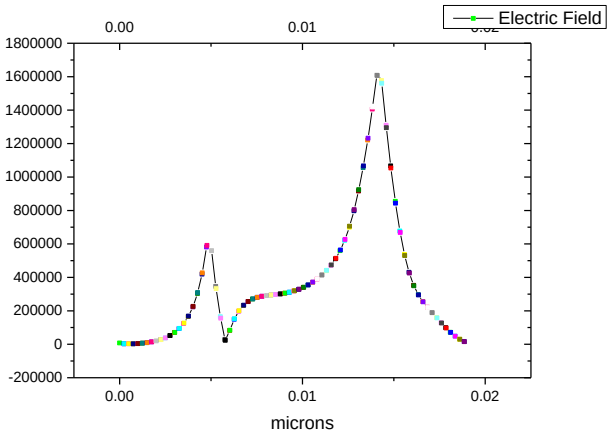

Figure 9: Graphical representation of the electric field

The diagram of electric field, E (V/cm) location toward the channel, x (nm) of GaN-based DG-MOSFETs for the gate length of 9.1nm for on state current.

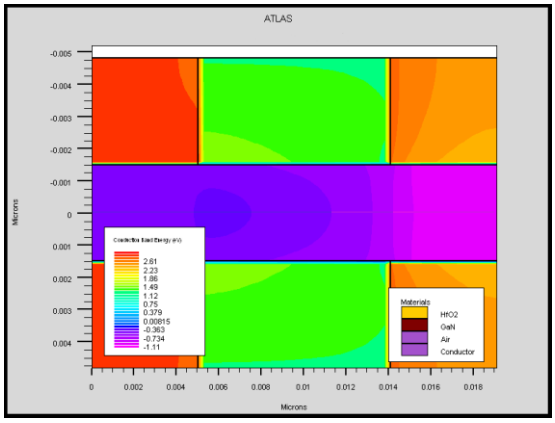

Figure 10: Conduction band energy for I_{ON}

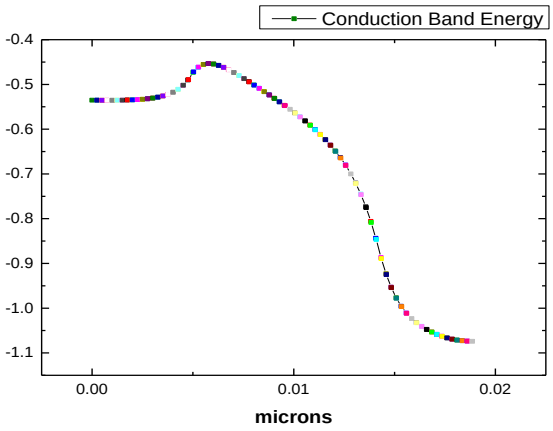

Figure 11: Graphical Representation of Band energy

Figures 11, shows the conduction band energy of GaN-based DG MOSFET and figure 8, demonstrates the graphical representation of conduction band energy for ON state current for the gate length of 9.1nm.

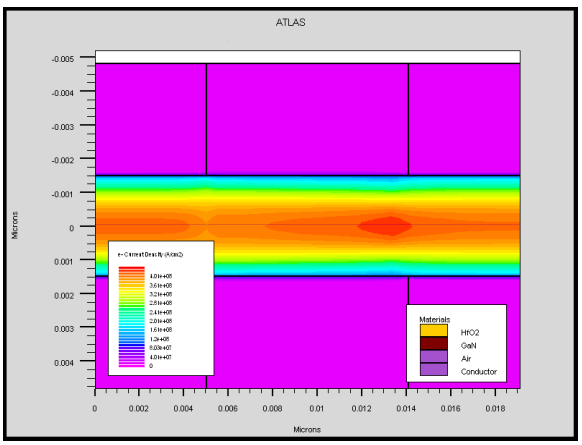

Figure 12: Electron current density

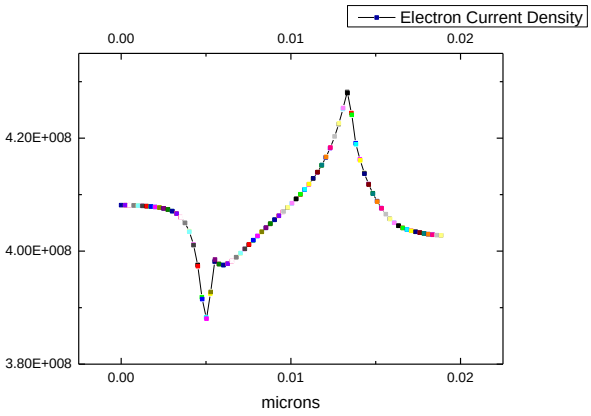

Figure 13: Electron current density

Figure 13 shows the electron current density of GaN DG MOSFET and Figure 10, demonstrates the graphical representation of electron current density.

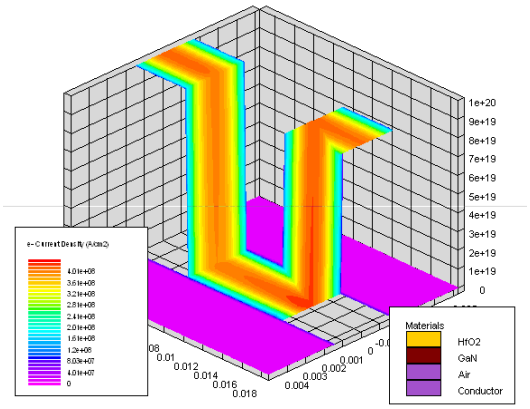

Figure 14: 3D view of GaN MOSFET

Figure 14, shows the 3D view GaN MOSFET of electron current density through a GaN-based DG MOSFET for L_G=9.1nm.

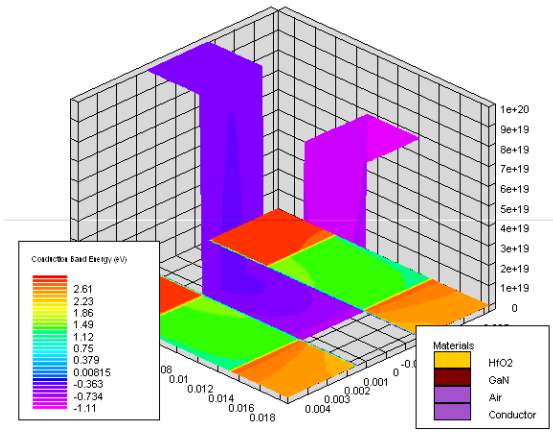

Figure 15: 3D view of GaN MOSFET

The above figure shows the 3D view of GaN MOSFET with respect to conduction band energy for the gate length of 9.1nm with V_{DS} =0.75V and V_{GS}=1V.

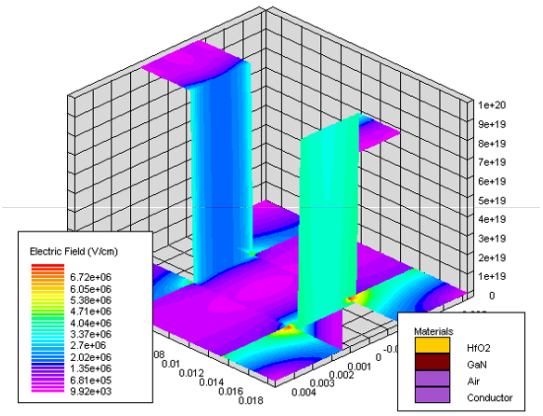

Figure 16: 3D view of GaN MOSFET for I_{OFF}

The above figure 16, shows the 3D view of GaN-based DG MOSFET for OFF-state current with L_G= 9.1nm, V_{DS}=0.75V, and V_{GS}= 1V.

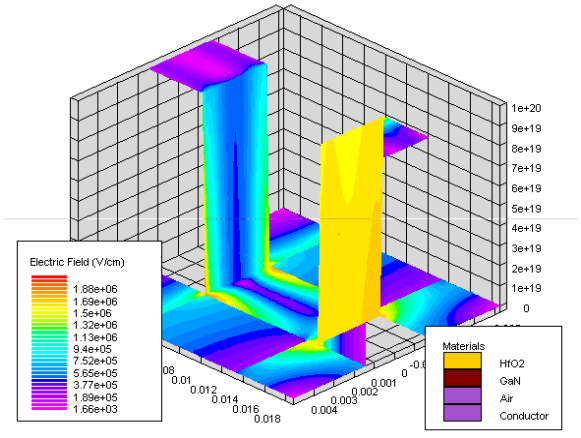

Figure 17: 3D view of GaN MOSFET for I_{ON}

Figure 17, shows the 3D view of GaN-based DG MOSFET for On state current with L_G= 9.1nm, V_{DS}=0.75V and V_{GS}= 1V. in this 3D view, it has been shown that. Channel is created between source and drain to conduct current for ON-state current and no channel is created for OFF-state current.

TABLE 3: Comparison with previous research GaN based DG MOSFET (IEEE:**7848446**) [24]

Description	Published results	Investigated results
Gate length	10.6nm	9.1nm
ON-state	V_{GS}=1V	V_{GS}=1V
V_{DD}	0.75V	0.75V
I_{ON}	11.4 mA/μm	12.1 mA/μm
SS	70.3mv/decade	69.3mv/decade
DIBL	96.5mv/V	31mv/V

Table 4: Comparison with GaN based DG MOSFET, **DOI: 10.1109/WIECON-ECE.2017.8468884 [25]**

Description	Published results	Investigated results
Gate length	10nm	9.1nm
ON-state	V_{GS}=1V	V_{GS}=1V
V_{DD}	0.75V	0.75V
I_{ON}	12 mA/μm	12.1 mA/μm
SS	69 mv/decade	69 mv/decade
DIBL	39 mv/V	31 mv/V

Table 5: Comparison with SI based SG MOSFET, **DOI: 10.1109/ICAEE.2017.8255445 [26]**

Description	Published results	Investigated results
Gate length	7.3nm	9.1nm
ON-state	V_{GS}=1V	V_{GS}=1V
V_{DD}	0.75V	0.75V
I_{ON}	11.7 mA/μm	12.1 mA/μm
SS	98 mv/decade	69.3mv/decade
DIBL	71 mv/V	31mv/V

Table 6: Comparison with SI based SG MOSFET, **DOI: 10.1109/ICAEE.2017.8255445 [27]**

Description	Published results	Investigated results
Gate length	9.3nm	9.1nm
ON-state	V_{GS}=1V	V_{GS}=1V
V_{DD}	0.75V	0.75V
I_{ON}	9 mA/μm	12.1 mA/μm
SS	78 mv/decade	69.3mv/decade
DIBL	47 mv/V	31mv/V

The above comparison tables represent the comparison between previous research results with our proposed device investigated results. The performance of GaN based DG MOSFET for the gate length of 9.1nm is compared with different gate length for GaN based DG MOSFET and SOI based SG MOSFET. The performance of GaN based DG MOSFET is efficient than the previous research results with respect to ON-state current, OFF-state current, Sub-threshold slope and DIBL

IV. CONCLUSIONS

The performance of GaN-based DG MOSFETs was investigated using Atlas Device Simulation Framework-Silvaco. The simulation results were precisely optimized in consideration of ON-state current, Subthreshold slope and Drain induced barrier lowering. The subthreshold slope was increasing with decreasing the gate length and shrinking the gate length increases the drain induced barrier lowering value. For better improvement, 2D and the 3D analytical figure has also been investigated for the electric field, conduction band energy and electron current density. Impressive results are found compared with previous research results. The overall performance of Si-based conventional MOSFETs will always be lower than GaN-based DGMOSFETs. GaN-based DG-MOSFETs is the most promising candidates for the future CMOS performance scaling.

REFERENCES

[1] Rupendra Kumar Sharma, Angelos Antonopoulos, Nikos Mavredakis, Matthias Bucher, "Analog/RF figures of merit of advanced DG MOSFETs", Devices Circuits and Systems (ICCDCS) 2012 8th International Caribbean Conference on, pp. 1-4, 2012.

[2] S. Panigrahy, P. K. Sahu, "Performance enhancement and reduction of short channel effects of nano-MOSFET by using graded channel engineering", Circuits Power and Computing Technologies (ICCPCT) 2013 International Conference on, pp. 787-792, 2013.

[3] Sharmistha Shee, Gargee Bhattacharyya, Subir Kumar Sarkar, "Quantum Analytical Modeling for Device Parameters and I – V Characteristics of Nanoscale Dual-Material Double-Gate Silicon-on-Nothing MOSFET", Electron Devices IEEE Transactions on, vol. 61, pp. 2697-2704, 2014, ISSN 0018-9383.

[4] M. R. Hasan, "Influence of device performance of Sub-10 nm GaN-based DG-MOSFETs over conventional Si-based SG-MOSFETs," 2017 4th International Conference on Advances in Electrical Engineering (ICAEE), Dhaka, Bangladesh, 2017, pp. 697-702. doi: 10.1109/ICAEE.2017.8255445.

[5] Noraini Othman, M. K. Md Arshad, S. N. Sabki, U. Hashim, "Impact of high-k dielectric on the digital and analog performance on emulation of double-gate UTBB SOI MOSFETs with different ground plane structures", Micro and Nanoelectronics (RSM) 2015 IEEE Regional Symposium on, pp. 1-4, 2015.

[6] Ankush Chattopadhyay, Arka Dutta, Atanu Kundu, Chandan K. Sarkar, "Influence on the analog/RF performance in graded channel Gate Stack DG-MOSFETs", Devices Circuits and Systems (ICDCS) 2016 3rd International Conference on, pp. 167-169, 2016.

[7] Huff, H. R., & Electrochemical Society. (2009). Into the nano era: Moore's law beyond planar silicon CMOS. Berlin: Springer.

[8] R. Nicole, "Title of paper with only first word capitalized," J. Name Stand. Abbrev., in press.

[9] D.K. Ferry, L.A. Akers, E.W. Greeneich, "Ultra Large Scale Integrated Microelectronics," Prentice-Hall, Englewood Cliffs, NJ, 1988

[10] Ieong M, Wong H S P, Nowak E, Kedzierski J and Jones E C "High performance double-gate device technology challenges and opportunities" Proc. Int. Symp. On Quality Electronic Design, 2002, pp.492–495.

[11] Bansal, B. C. Paul, and K. Roy, IEEE Trans. Electron. Dev. 52, 256 (2005).

[12] Z. Ren, R. Venugopal, S. Datta, M. Lundstrom, D. Jovanovic, J. Fossum, IEDM Tech. Dig. (2000) 715.

[13] M. Balaguer, B. Iñíguez, and J. B. Roldán, "An analytical compacmodel for Schottky-barrier double gate MOSFETs,"Solid-State Electron., vol. 64, no. 1, pp. 78–84, 2011.

[14] T. Sekigawa, Y. Hayashi, Solid-State Electron. 27 (1984) 827.

[15] Kranti, T., M. Chung, and J.-P. Raskin, "Analysis of static and dynamic performance of short channel double gate SOI MOSFETs for improved cut-off frequency," Jpn. J. Appl. Phys. , vol. 44, no. 4B, 2005, pp. 2340-2346.

[16] Raseong Kim, Avci UE, Young IA. Comprehensive Performance Benchmarking of III-V and Si nMOSFETs (Gate Length=13 nm) Considering Supply Voltage and OFF-Current. IEEE Trans Electron Devices. Mar 2015; 62: 713–721p.

[17] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFETs with very small physical dimensions," IEEE J. Solid-State Circuits, vol. SC-9, pp. 256–268, Oct. 1974.

[18] D. L. Critchlow, "MOSFET scaling—The driver of VLSI technology,"Proc. IEEE, vol. 87, pp. 659–667, Apr. 1999.

[19] [Y.-K. Choi, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "Sub-20 nm CMOS FinFET technologies," in Tech. Dig. IEDM, 2001, pp. 421–424.

[20] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, "High performance fullydepleted tri-gate CMOS transistors," IEEE Electron Device Lett., vol. 24, no. 4, pp. 263–265, Apr. 2003

[21] Z. Ren, R. Venugopal, S. Datta, M. Lundstrom, D. Jovanovic, J. Fossum, IEDM Tech. Dig. (2000) 715.

[22] M. Balaguer, B. Iñíguez, and J. B. Roldán, "An analytical compacmodel for Schottky-barrier double gate MOSFETs,"Solid-State Electron., vol. 64, no. 1, pp. 78–84, 2011.

[23] Md. Rokib Hasan, Md. Saud Al Faisal, Marwan Hossain and Mohammad Saiful Islam. "Effect of Underlap on Device Performance of GaN based DG-MOSFET". LAMBERT Academic Publishing (LAP) (2016-07-26).Project-ID (141341) and the book's ISBN (978-3-659-92013-4).https://www.morebooks.de/store/gb/book/effect-of-underlapon- device performance-of-gan-based-dg-mosfet/isbn/978-3-659-92013

[24] IEEE. (2018). [online] Available at: https://ieeexplore.ieee.org/document/7848446 [Accessed 24 Dec. 2018].

[25] Hasan, Md. Rokib, et al. "Gate Length Engineering Impact of Sub-10 Nm GaN-Based DG-MOSFETs." *2017 IEEE International WIE Conference on Electrical and Computer Engineering (WIECON-ECE)*, 2017, doi:10.1109/wiecon-ece.2017.8468884.

[26] Hasan, Md. Rokib. "Influence of Device Performance of Sub-10 Nm GaN-Based DG-MOSFETs over Conventional Si-Based SG-MOSFETs." *2017 4th International Conference on Advances in Electrical Engineering (ICAEE)*, 2017, doi:10.1109/icaee.2017.8255445.

[27] Hasan, Md. Rokib. "Influence of Device Performance of Sub-10 Nm GaN-Based DG-MOSFETs over Conventional Si-Based SG-MOSFETs." *2017 4th International Conference on Advances in Electrical Engineering (ICAEE)*, 2017, doi:10.1109/icaee.2017.8255445.

MD. Rabiul Islam received his Bachelor and master's degrees in Electrical and Electronic Engineering from American International University-Bangladesh (AIUB). His research interest is nano-electronics. He is currently working as a Lecturer under the department of Faculty of Engineering, American International University-Bangladesh.

Md. Rokib Hasan received the B. Sc. in Electrical and Electronics Engineering from the American International University Bangladesh (AIUB), Bangladesh, in 2016. His research interests include semiconductor device physics, modeling and simulation design and power electronics. Currently, he is working as Electrical Engineer in the Department of Inspection for Factories and Establishments (DIFE) under Ministry of Labor and Employment (MOLE) on Remediation Coordination Cell (RCC) Project.

Dr. Md. Kamrul Hassan received his B.Sc. degree in Electrical and Electronic Engineering from Bangladesh University of Engineering and Technology, (BUET), Dhaka in 1987 and Dr. of Engineering degree in Plasma Science and Engineering (Plasma Deposition & Electrical Characterization of Diamond-Like Carbon (DLC) Thin Films) from Kochi University of Technology, Japan, in 2007.He started his professional career as an Assistant Engineer (Electrical/Instrument) in Bangladesh Chemical Industries Corporation (BCIC) from September, 1988, became an Executive Engineer in 1997. During his job in BCIC, he also completed Post-Graduate Diploma in Industrial Management (PGDIM) in 1990 from Bangladesh Management Development Centre, Dhaka, Bangladesh. He also completed many training courses on different types of process control instrumentations including programmable logic controller (PLC) and programmable instruments during his job in BCIC from 1988 to 2003.
After having the Dr. of Engineering degree, he started his teaching career as an Assistant Professor in Electronic and Telecommunication Engineering (ETE) Department of Daffodil International University, Dhaka, Bangladesh in May, 2008 and he worked there till August, 2008. On September, 2008, he joined as a Faculty member of Electrical and Electronic Engineering (EEE) Department under Engineering Faculty, American International University-Bangladesh (AIUB). On May, 2009 he was appointed as an Assistant Professor of EEE Department, Faculty of Engineering, AIUB. Currently he is an Associate Professor at the American International University-Bangladesh (AIUB). His present research interest includes Plasma Science, Nanotechnology, Electrical Characterization of Nanostructure Thin Films, and Solid state electronics, Materials science. Dr. Md. Kamrul Hassan is a Member of the Institution of Engineers Bangladesh (IEB).

Mohammad Abdul Mannan was born in Laxmipur, Bangladesh on January 01, 1975. He received his B. Sc. Eng. Degree from Rajshahi University of Engineering and Technology (RUET former BITR), Bangladesh, in 1998, and Masters of Eng. and Dr. of Eng. degrees from Kitami Institute of Technology, Japan, in2003 and 2006 respectively , all in Electrical Engineering. He then joined American International University Bangladesh (AIUB) as an Assistant professor. At present he is Professor & serving as Under Graduate Head of EEE department in American International University- Bangladesh (AIUB). He is a member of the IEEE and IEB. His research interests include electric motor drive, power electronics, power system, wind generation system and control of electric motor, power electronic converters, power system, and wind generation
system.

M. Tanseer Ali received Doctor of Engineering degree from University of Greenwich (UK), 2013. His research interest is focused on Analog Electronics, RF/Microwave Circuits and Systems, Nano-electronics, Nuclear Power, Solid State Circuits. Currently he is working as Senior Assistant professor in the department of EEE, AIUB