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Effects of Doping Concentration on Device Performance of GaN-based Nano-regime MOSFETs

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***Abstract*—-Gallium nitride (GaN) based metal-oxide semiconductor field-effect transistors (MOSFETs) are promising for switching device applications. The doping of n- and p-layers is varied to evaluate the figure of merits of proposed devices with a gate length of 10 nm. Devices are switched from OFF-state (gate voltage, VGS = 0 V) to ON-state (VGS = 1 V) for a fixed drain voltage, VDS = 0.75 V. The device with channel doping of 1×10^{16} cm^{-3} and source/drain (S/D) of 1×1020 cm-3 shows good device performance due to better control of gate over channel. The ON-current (I_{ON}), OFF-current (I_{OFF}), subthreshold swing (SS), drain induce barrier lowering (DIBL), and delay time are found to be 6.85 mA/µm, 5.15×10^{-7} A/µm, 87.8 mV/decade, and 100.5 mV/V, 0.035 ps, respectively. These results indicate that GaN-based MOSFETs are very suitable for the logic switching application in nanoscale regime.**

Keywords*— *GaN; MOSFET; Digital Logic Application; Doping concentration; Nanoscale;

I. INTRODUCTION

For future logic switching devices, it is necessary to shrink up the devices in nanoscale regime [1]. However, fabrication of the traditional semiconductor such as Si and Ge based transistors have become more and more difficult to shrink in size up to the breakdown point of the atomic size barrier [2-5]. The fact implies a fundamental size limit on the atomic/nucleus scale and it is difficult to maintain the logic application as it snags from the certain precincts [6-7]. Since fabrication of the first MOSFET, length of the channel has been shrinking continuously. The primary goal of scaling of the MOSFET is to achieve the high-speed and high-efficiency; nonetheless it may create issues regarding saturation velocity, degradation of mobility, leakage currents, and breakdown voltages [8]. The motivation behind the miniaturization of devices has been an increasing interest in the high-speed devices and very large scale integrated circuits. To meet the future demand, the selection of new channel materials with miniature structures is highly required. Therefore, the proper usage of material and structural parameters, such as doping concentration, choosing of gate oxide, effective-oxide thickness (EOT), channel length, channel thickness etc., are obligatory for the fabrication of devices in nano-scale regime. It is very well known that GaN is very suitable for the choice as a channel material due to its inherent properties such as lower effective mass, high electron, high saturation velocity [4]. To upgrade the carrier mobility in a channel and to control the threshold voltage and drive current [10-13], the fabrication of MOSFET is focusing on the doping of source/drain and channel/body coming out from the thinking of intrinsic doping channel. As, intrinsic channel MOSFETs need to rely solely on gate work-function to achieve multiple threshold voltages on a chip due to the absence of channel/body doping. In this case, it is an efficient tool to adjust the threshold voltage in MOSFETs with doped source and drain [14, 15]. Doping concentration offers the easiest way to increase the drive current for specific applications. Therefore, GaN-based MOSFETs with suitably doping concentration seem to be the easiest option from a fabrication point of view, and are seriously being investigated to set appropriate threshold voltages and achieving the desired output for specific logic application [16-18]. With the high doping concentration near the source/drain junction depth, several parameters, like the carrier mobility, drain current are set on desire values and channel/body doping concentration is kept low and act like a tuner to fine the Short Channel Effects SCEs to achieve an extreme retrograde doping profile. Although heavy channel doping can suppress SCEs to some extent and fix threshold voltage, it has already been established that such high doping will rigorously degrade the mobility in the channel because of the increasing ionized impurity scattering, the resistance from source to drain increases [18] and the increase of time to form a channel under the gate oxide with the applied gate voltage known as delay time, and will contribute to threshold voltage roll off resulting from the significant discrete dopant fluctuation effect [19].

In this paper, ultra-thin body GaN-based MOSFETs with a gate length, LG of 10 nm and a high-k (HfO_2). The performance parameters of GaN-based MOSFETs, which are operated in enhancement mode, have been evaluated for optimizing the doping concentration in all regions (source, channel and drain). The source/drain (S/D) doping concentrations are varied from 1×10^{19} cm^{-3} to 1×10^{21} cm^{-3} with a fixed channel/body doping concentration of $1\times10^{16}/cm^{-3}$. Again the channel/body doping concentrations are varied from 1×10^{16} cm^{-3} to 1×10^{19} cm^{-3} with a constant and source/drain (S/D) doping concentration of 1×10^{20} cm^{-3}. The source to drain voltage, VDS is fixed at 0.75 V. The figure of merits such as I_{ON}/I_{OFF}, DIBL, SS, and delay time has also been evaluated. The drain current is normally calculated by quantum mechanical approaches. The simulation is based on the self-

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consistent solution of the 2-D Poisson equation and Schrodinger equation with open boundary conditions within the non-equilibrium Green's function (NEGF) formalism. All the calculations have been done at room temperature.

II. Device Structure

The schematic diagram of GaN-based MOSFET is shown in Figure 1. The device dimensions and material parameters are shown in the Table 1. The electron effective mass is considered as 0.18 m0 which is based on effective mass approximation method. The simulation has been done in SILVACO Atlas platform.

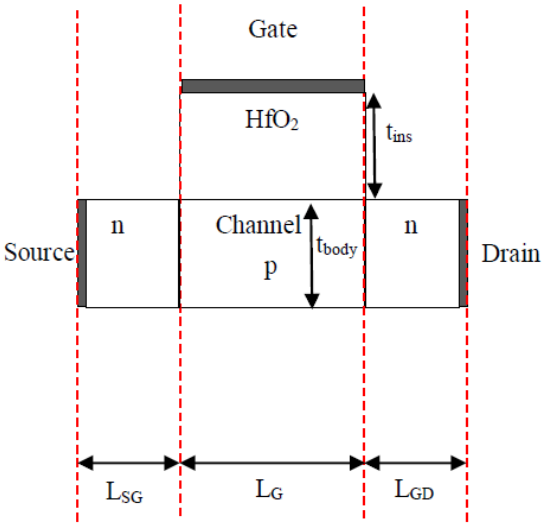

Fig. 1. Cross-sectional view of GaN based single gate MOSFET.

TABLE I. Parameters used in the simulation of the Device Structure.

Para-meters	Value	Description
ε_{ins}	22	HfO_2 as gate oxide
t_{body}	3 nm	Thickness of the channel used
t_{ins}	2.82 nm	Thickness of HfO_2/ZrO_2 gate oxide, Equivalent oxide thickness (EOT)= 0.50 nm
L_G	10 nm	Gate length (region right below the gate oxide)
$L_{SG/GD}$	5 nm	Extension of the channel towards source and drain along each side
N_{body}	P-type, 10^{16}-10^{19} cm^{-3}	Doping at the L_G region
$N_{SG/GD}$	N-type,10^{19}-$10^{21}cm^{-3}$	Doping at the each $L_{SG/GD}$ region

III. Results and Discussion

Figure 2 shows the conduction band profile of the proposed GaN-based nanoscale MOSFETs during ON-state (VGS = 1 V) for different doping concentration of S/D Figure 2 (a) and channel Figure 2 (b). The continuous increasing of source/drain doping concentration with a fixed channel doping of 10^{16} cm^{-3}, the barrier height become as much higher that create a barricade to flow electron from source to drain but the width of the barrier starts to decrease and electron can also bounce back/tunnel from drain to source easily that is causing SCEs. In Figure 2 (a) the channel doping has been kept fixed at 10^{16} cm^{-3} and the source/drain doping has been varied. For S/D doping concentration 1×10^{19} cm^{-3} the source and drain is in tunneling domain region. The gate voltage has lost control over channel. In Figure 2 (b) the S/D doping has been kept fixed and channel doping has been increased that causes not only the height of the barrier, but also the extension of the barrier in the channel along the transport direction where it is greater than the potential level of the source increases. For a higher body doping concentration of channel region with a fixed S/D doping concentration, the height of the potential barrier is increasing.

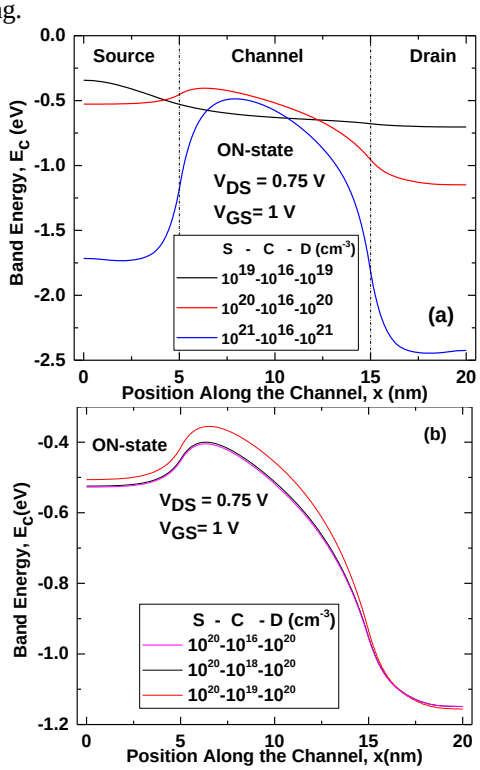

Fig. 2. (a) Potential energy profile along the channel for varying source/drain doping concentration (10^{19}-10^{21} cm^{-3}). (b) Potential energy profile along the channel for varying channel/body doping concentration (10^{16}, 10^{18}, and 10^{19} cm^{-3}). the source/drain doping is kept fixed (10^{20} cm^{-3}) in both (a) and (b).

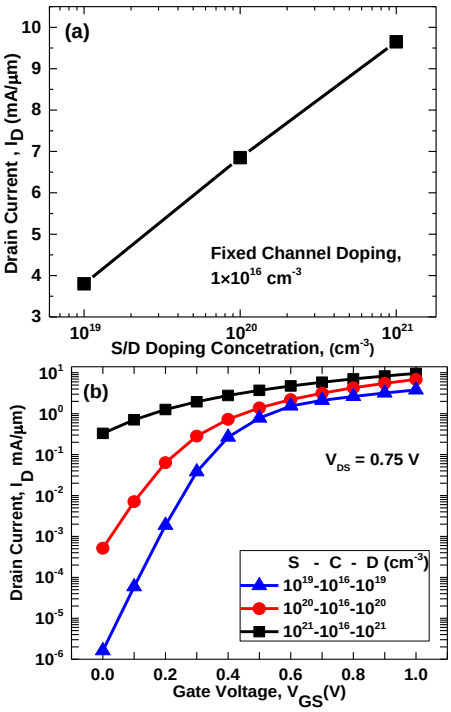

Fig. 3. (a) Drain current (ID) versus variable S/D doping concentration at VDS = 0.75 V. (b) Drain current (ID) versus gate voltage (VGS) for different S/D doping in log scale at VDS = 0.75 V. (Channel doing has kept fixed on 10^{16} cm^{-3}).

However, the conduction band profiles are almost same for the channel doping 10^{16} and 10^{18} cm^{-3}. These results indicate that this increase in the height as well as width of the potential barrier with p-doping exponentially reduces source-to-drain tunneling, and accounts for the sharp decrease in the leakage current when the transistor is OFF-state. The challenge is to choose an optimum doping concentration that is able to meet the requirement of high performance (HP), high speed and low standby power consumption for digital switching with the lowest amount of SCEs.

In Figure 3 the transfer characteristic of the GaN-based MOSFEET for various S/D doping is shown. The Figure 3 (a) depicts that an increasing in drain current with the increasing in doping at the each LSG/GD region for a fixed doping at the LG region. The highest drain current, 9.65 mA/μm is obtained from S/D doping 1021 cm-3. The Figure 3 (b) depicts that an increasing in OFF-state current from 1.61×10-9 A/μm to 3.3x10-4 A/μm with the increasing in doping at the LSG/GD region from 1019 cm-3 to 1021 cm-3 for a fixed LG doping region. With an increase of the S/D doping, the barrier width is decreasing, so the OFF-state current has been increased. For a fixed gate voltage, the concentration of the channel/body doping controls the height of the source to channel barrier; it is clear that with an increment of the body doping concentration at the p-region, the electron inversion is weak; therefore the on current is decreased.

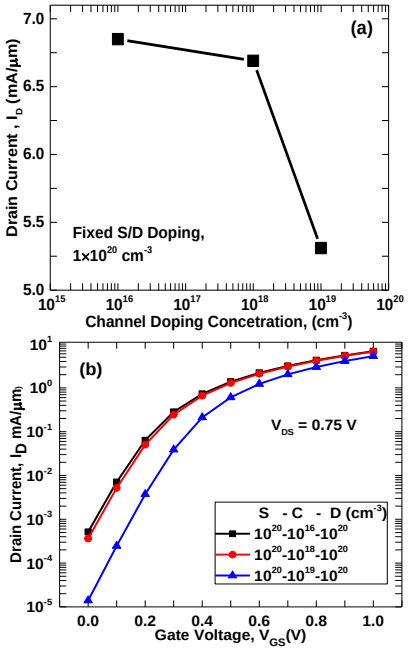

Fig. 4. (a) Drain current (ID) versus variable Channel doping concentration at VDS = 0.75V. (b) Drain current (ID) versus gate voltage (VGS) for different channel doping in log scale at VDS = 0.75 V. (S/D doing has kept fixed on 10^{20} cm^{-3})

Figure 4 (a) depicts that a decreasing in drain current from 6.85 mA/μm to 5.31 mA/μm with the increasing in doping at the LG region for a fixed doping at the each LSG/GD region. The Figure 4 (b) depicts that a decreasing in OFF-state current from 5.15×10^{-7} A/μm to 1.39x10^{-8} A/μm with the increasing in doping at the LG region for a fixed LSG/GD doping at the region. Moreover, a substrate with specific (or added) body doping is sometimes needed when a threshold voltage adjustment is required. The subthreshold swing (SS) characteristics are shown in Figure 5. The subthreshold region shows in Figure 5 (a) that the tendency of steeper and smoother slope for higher body doping and the decreasing level in the higher S/D concentration shows in Figure 5 (b).

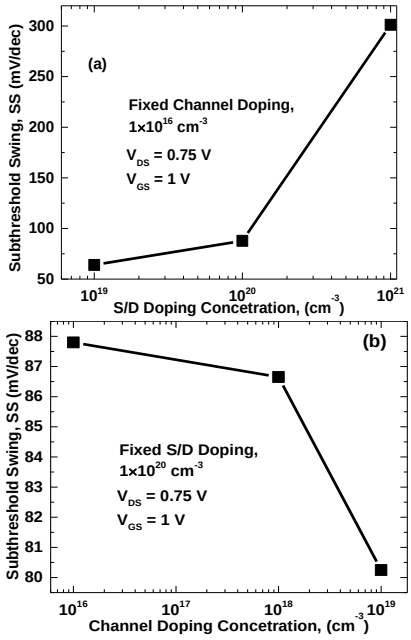

Fig. 5. Dependence of SS with the change of (a) S/D doping concentration (Fixed Channel doping $10^{16}cm^{-3}$) (b) Channel doping concentration (Fixed S/D doping 10^{20} cm^{-3}).

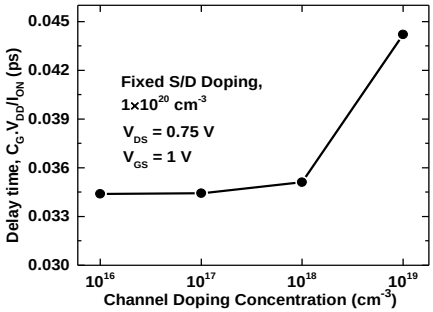

Fig. 6. Variation of intrinsic gate delay with the change of channel doping concentration. (S/D doping is fixed at 10^{20} cm^{-3})

Because by increasing the body doping concentration, although both the on-current and off-current are decreasing at higher body doping, but the rate of reduction in the off-current is faster than the on-current. Table 2 shows the drain induced barrier lowering (DIBL) effects on the GaN-based MOSFET for S/D and channel doping concentration. Table 2 (a) shows that the DIBL increase with the increasing of S/D doping that indicates, the gate is losing control over channel. For doping concentration below 1019 cm-3 the channel is in tunneling domain region for that the DIBL is higher for S/D doping below 1019 cm-3. Table 2 (b) shows the DIBL decrease with the increase of channel/body doping concentration. For increasing channel doping concentration, there is a reduction of CG, the increase series resistance, the ION and hence increase gate delay (CG.VDD/ION) of the device shown in Figure 6. The S/D doping has been kept fixed on 1020 cm-3 and varied the channel/body doping concentration.

IV. CONCLUSION:

Because of excellent transport properties, large direct band gap, high saturation velocity, large conduction band discontinuities, high thermal stability, strong spontaneous and piezoelectric polarization effect, GaN material is a promising candidate of replacing Si from the channel. GaN as a channel material has already been considered for regular channel devices and proved its superiority. But for nano-scale devices, it is not premeditated in detail. In this paper, the performance of GaN-based nanoscale MOSFETs for gate length LG = 10 nm is simulated using NEGF method for the S/D region and channel doped varied from 10^{19} cm^{-3} to 10^{21} cm^{-3} and 10^{16} cm^{-3} to 10^{19} cm^{-3}, respectively.

TABLE II. SIMULATION RESULTS ACCUMULATION. (A) FOR VARIABLE S/D DOPING (B) FOR VARIABLE BODY DOPING.

Parameters **(a)**	**Doping Concentration** **Fixed channel doping $1x10^{16}cm^{-3}$** Variable S/D doping		
	$1x10^{19}$ cm^{-3}	**$1x10^{20}$ cm^{-3}**	**$1x10^{21}$ cm^{-3}**
I_{ON}(mA/μm)	3.80	6.85	9.65
I_{OFF} (A/μm)	$1.61x10^{-9}$	$5.15x10^{-7}$	$3.3x10^{-4}$
I_{ON}/I_{OFF}	$2.35x10^{6}$	$1.33x10^{4}$	$2.9x10^{1}$
SS (mV/dec)	64	87.8	301.2
DIBL(mV/V)	130.67	100.5	348.7

Parameters **(b)**	**Doping Concentration** **Fixed S/D doping $10^{20}cm^{-3}$** Variable Channel doping		
	$1x10^{16}$ cm^{-3}	**$1x10^{18}$ cm^{-3}**	**$1x10^{19}$ cm^{-3}**
I_{ON} (mA/μm)	6.85	6.69	5.31
I_{OFF} (A/μm)	$5.15x10^{-7}$	$3.62x10^{-7}$	$1.39x10^{-8}$
I_{ON}/I_{OFF}	$1.33x10^{4}$	$1.84x10^{4}$	$3.8x10^{5}$
SS (mV/dec)	87.8	86.65	80.25
DIBL(mV/V)	100.5	118.8	125

To treat the carrier reflection accurately, source drain contacts are allowed to float. From the Table-2, it is clear that the drain current (9.65 mA/μm) increases with the increase of S/D doping (10^{21} cm^{-3}), which implies that the gate gradually loses control over the channel and short channel effects (SCEs) become more prominent (SS = 301.2 mV/decade and, DIBL = 348.7 mV/V). Body doping has used to overcome those SCEs. The best suited doping concentration for 10 nm GaN-based MOSFET is 10^{20} cm^{-3} for S/D and 10^{16} cm^{-3}. So, for future application of GaN-based MOSFETs devices, one needs to optimize the I_{ON} /I_{OFF} and SS values for specific digital logic designs.

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