A Novel Transformer-less Grid Tie Inverter for Rooftop PV system

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Abstract— **This paper presents a relatively new concept for the design and implementation of a grid-tie inverter for photo voltaic (PV) systems. The proposed method will eliminate the uses of battery pack hence overall cost of any PV project will be significantly reduced. As the output of any PV array varies with the variation of solar irradiance hence a boost converter with PID regulated variable duty cycle has been used to keep a constant input to the inverter. Multilevel inverter topology has been proposed for utility grid connectivity. The proposed design is simulated in MATLAB/Simulink and a prototype is also implemented to verify the simulation results. The controllers are implemented in Arduino microcontroller board.**

Index Terms—**PV array, PID controller, multilevel inverter, gate driver, PWM technique.**

I. INTRODUCTION

Fossil fuels such as oil or natural gas along with some non-commercial fuels are considered as the main resources around the world. It is predicted that the global electricity generation will increase to 31.8 trillion kWh by the year 2021 [1]. With its increasing demand, the search for energy resources other than fossil fuels has become momentous. Solar, wind and hydro are renewable energy sources that are seen as reliable alternatives to this conventional energy sources. These alternatives also eliminate the emission of harmful carbon dioxide and other greenhouse gases, unfavorable to the environment. Thus, few countries around the world aims to achieve 20% of total generated electricity from renewable energy sources by the year 2020. This is believed to be accomplished through grid-connected wind farms and solar photo-voltaic (PV) systems [2].

With the rapid growth of worldwide economic, the demand of the electricity increase excessively. Grid-connected PV generation have gained popularity as it promotes green energy sources [3-4]. Conventional grid connected PV inverter systems typically use transformers to step up or down voltages extracted from the converters; this make the schemes indubitably expensive [5]. The utmost fact about the installation of PV panel for large scale application is the significant cost of battery pack. Several studies found that battery costs almost 50% budget of a PV project. Moreover, battery needs frequent maintenance.

Many researchers proposed CUK and SEPIC converter [6-7] for grid connected PV system. But their design is based on open loop control strategy hence the output voltage of the converter will not be constant with the variation of the solar irradiance. Many inverter topologies such as H6, HERIC, HB-ZVR, NPC have been proposed in the literature. But these topologies are based on the structure of freewheeling path of anti-parallel diode [8-15]. As a result, diode conduction loss will occur during each switching period [16]. The multilevel inverter does not work on the structure of freewheeling path of anti-parallel diode which results lower conduction losses during switching [17]. The proposed system uses a multilevel inverter with a regulated PID controller to generate the duty cycle of the boost converter. As a result, it will be possible to keep the output voltage of boost converter constant for varying solar irradiance. Also the proposed system will eliminate the use of battery pack and transformer for step up-down operation which will ultimately save a significant cost. Using the conventional rooftop PV system, the capital cost is much higher. As a result, many people are not interested in installing PV arrays on their rooftop. But using the proposed system, the power from the PV arrays will be directly connected to the grid rather storing in a battery pack. Thus, installing rooftop PV arrays will be much cheaper and simpler which will encourage more people to install PV arrays on their rooftop.

II. DESIGN SPECIFICATION

The basic topology proposed in this paper is given in fig. 1 where a PV panel, a boost converter and multilevel H bridge inverter are designed which is simple in construction. In this proposed system, the PV array is sized in such a way that it can provide nearly

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110V to the converter. A sinusoidal based pulse width modulation is also proposed to control the gate pulse of the MOSFETs. In order to ease maximum power efficiency a gate driver circuit is proposed which in turns also accomplishes the purpose of the isolation of the MOSFET in multilevel inverter. So this proposed system is also reliable and noiseless.
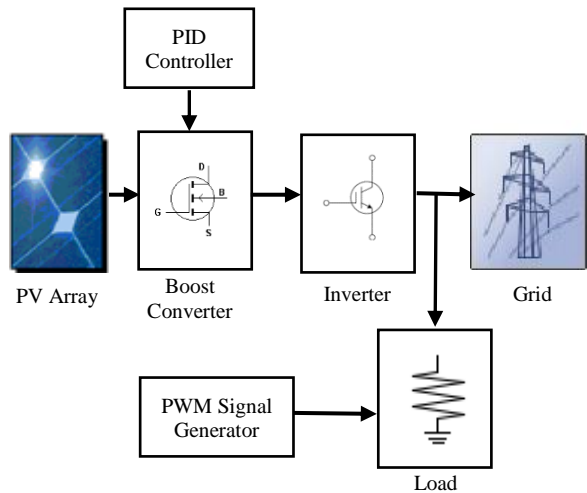

Fig. 1. Transformer less grid connected PV inverter without storage

III. CONVERTER DESIGN

Converter is an electromechanical device, which receives the DC voltage from different sources and converts the voltage level to higher or lower as needed. The converter also provides isolation between input source and load when required. It is also used to protect supplied system and the input source from electromagnetic interference (EMI). To design a DC to DC boost converter, few specifications are followed based on application such as the conversion of voltage ratio range, power conversion efficiency, power density, the maximal output power, number of components etc. But for PV system application, power density and number of components are not design constrain as the required area for the converter is not a vital issue. As the objective is to connect the power generated by the rooftop PV panel to the domestic grid hence the maximum output voltage should be 600V. As generating more than 15kW power by using rooftop PV panel is not realistic hence the power rating of the converter should be 15kW.

The purpose of using the DC to DC boost converter is to regulate switching mode DC power supplies. The input of the converter is an uncontrolled DC voltage, comes from the PV array and PID controller is used to obtain the desired value although the input voltage is fluctuating. The average output voltage is controlled by a switch on and off duration.

$$V_{out} = V_{in} / (1-D) \qquad (1)$$

To obtain a constant frequency, the on-off duration of the switch is adjusted; the switching duty cycle D is defined as the ratio of time a load or circuit in ON compared to the time the load or circuit is OFF. Fig. 2

illustrates the initial action of the converter circuit at continuous conduction mode, when the gate pulse is given to the MOSFET is high means the power MOSFET is switched on at t=0 to t=t_{on}. The high frequency square wave turns on the MOSFET and executes a short circuit with the inductor. So the current flows in between the supply side and creates a magnetic field on inductor. Due to the magnetic field, inductor stores energy linearly. So the inductor current $I_L(t)$ also increasing and The inductor voltage is V_L.
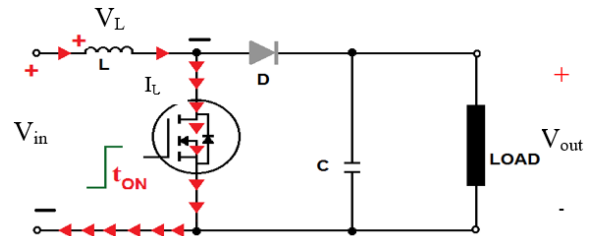

Fig. 2. Initial conduction mode of converter

Fig. 3 represents the off period condition of the converter circuit. The low signal at the gate turns off the MOSFET and the current through the inductor provides a negative polarity. Hence the output voltage, $V_{out} = V_{in}+V_L$. Considering that the MOSFET is turned on and off for t_{on} and t_{off} time duration respectively, the voltage equation can be written as-

$$V_{in}(t_{on} + t_{off}) = V_{out} \times t_{off} \qquad (2)$$

$$V_{in} \times T_s = V_{out} \times t_{off}$$

$$\frac{V_{out}}{V_{in}} = \frac{T_s}{t_{off}} = \frac{1}{1-D} \qquad (3)$$

Where, T_s is the switching period and D is the duty cycle. Thus, V_{out} is inversely proportional to (1-D) it is obvious that the duty cycle, D, cannot be equal to 1 otherwise there would be no energy transfer to the output assuming a lossless circuit, $P_i=P_o$.
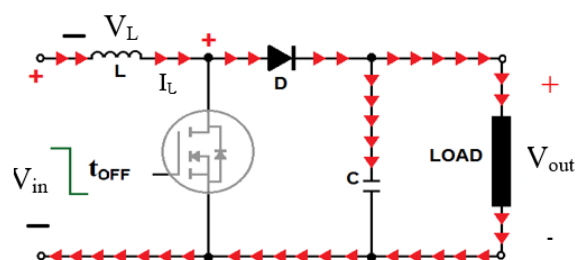

Fig. 3. Off period conduction of the converter circuit

Fig. 4 shows the scenario after finishing the first cycle of the square wave. So the high frequency square wave again provides to the MOSFET gate and it again creates a short circuit path at the supply side with the inductor. The inductor stores energy because of the magnetic field. But this time the operation at the output part is changed. The capacitor at the output side starts

discharging through the load and the diode here provides isolation between the input part and the output part. At the off period the capacitor charged each time and this process maintains the output voltage each time through load.
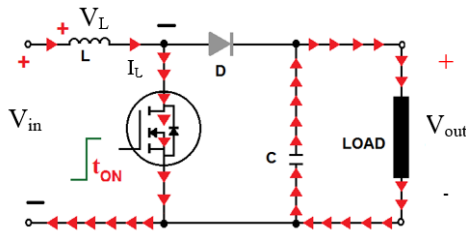

Fig. 4. On period conduction of the converter circuit

The required duty is generated from a PID controller which is discussed in later section.

IV. INVERTER DESIGN

Multilevel inverter topology has been chosen because it needs less filter components which results in reduced cost and weight of the inverter [18]. Proposed scheme of inverter is shown in fig. 5. Two pair of switches turn on simultaneously. 120^0 conduction mode has been used in the design of the inverter. During the first 120°, S_1 conducts with S_6 for 60° then again conducts with S_2 for another 60°. The S_3 will conduct for 120° (from 120° to 240°) where 60° (from 120° to 180°) with S_2 and another 60° with S_4 (from 180° to 240°). The S_5 will conducts 120° (from 240° to 360°) where 60° with S_4 (from 240° to 300°) and another 60° (from 300° to 360°) with S_6. The conduction sequence can be written as follows: S_6S_1, S_1S_2, S_2S_3, S_3S_4, S_4S_5, S_5S_6 and S_6S_1.
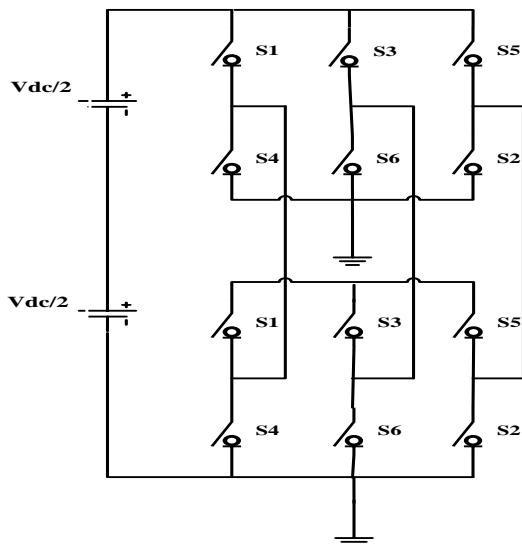

Fig. 5. Design of the inverter

Fig. 6 represents the switching signals and corresponding line to neutral and line to line voltage.
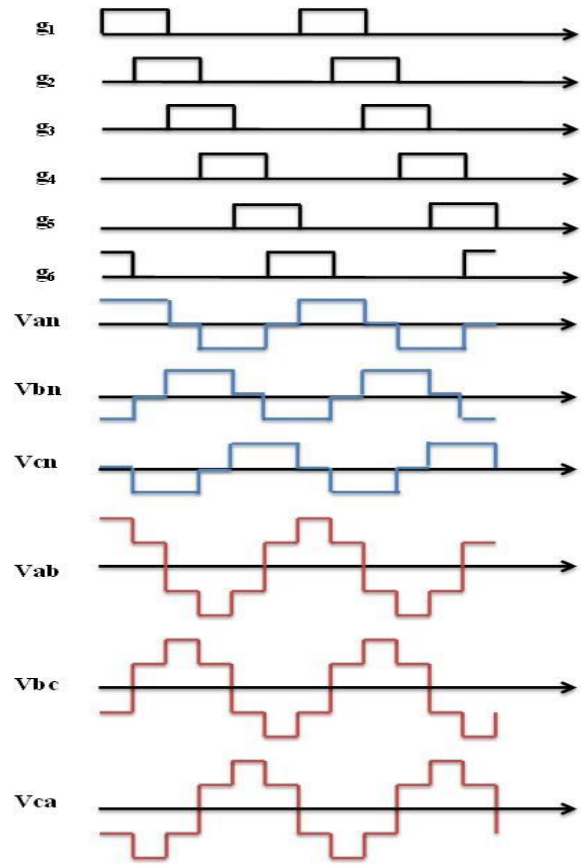

Fig. 6. 120^0 conduction mode

V. CONTROLLER DESIGN

The controller is the unit designed to create a stable close loop system and static process performance requirement. The input of the controller unit is basically an unbalanced and error signal based on the difference between the measurement of output and a desired set-point or reference signal.

A. PID Controller

The PID controller makes the close loop system stable. For the disturbance in the process, the controller may have disturbance rejection object which plays the role to attain the reference tracking object. The PID controller also carries the attenuation property for filtering the noise signals of the measurement process. It makes the nonlinear process to linear and steady state operation [19-20].

A basic block diagram of PID controller is shown in fig. 7, where the Proportional gain $K_P = 0.65$, the Integral gain $K_I = 150$ and the derivative gain $K_D = 2.7e^{-6}$ is taken for the PID used in the proposed design.
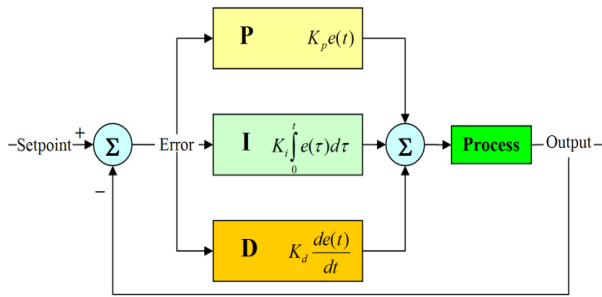
Fig. 7. Basic block diagram of PID controller

Its transfer function can be written as,

$$G(s) = K_P + K_I (1/S) + K_D s$$
$$= K_P [1 + (1/ T_I s) + T_D s] \qquad (4)$$

Where,

K_P = Proportional gain

K_I = Integral gain

K_D = derivative gain

T_I = Integral time constant

T_D = Derivative time constant

Proportional control: This proportional term formed when the controller action being proportional to the size of the process error signal. The time and Laplace domain represents the mathematical term of the proportional control.

Time domain: $A(t) = Kp \times e(t)$
Laplace domain: $A(s) = Kp \times E(s)$

Integral control: The proportional term intends to reduce the overall error with time but it's not able to reduce the error level to zero and there are always some steady state errors in the system. Integral control overwhelms the limitation of the proportional control by eliminating the steady state error without the use of excessively large controller gain. The mathematical term of Integral control represents by time and Laplace domain.

Time domain: $A(t) = Ki \int_0^t e(t)\, d(t)$

Laplace domain: $A(s) = \left[\dfrac{Ki}{s}\right] E(s)$

Derivative control: This term uses the rate of change of the error signal, then acquaint with a predict element into control action. The derivative term assists to improve the transient response through high-frequency compensation by a differentiator. Mathematically, the time and Laplace domains are,

Time domain: $A(t) = Kd \times \dfrac{de(t)}{d(t)}$
Laplace domain: $A(s) = K_d s \times E(s)$

B. Gate driver Circuit

Power semiconductor devices have three operating states which are commonly known as the cut-off, the active and the saturation mode. The aim of converters

in power electronics which utilize switch mode operation is to operate these converters in either the saturation or the cut-off region. A gate driver is a power amplifier that accepts a lower power input from a controller IC and produces the appropriate high-current gate drive for power MOSFET. A gate driver is thus used when a pulse-width-modulation (PWM) controller cannot provide the output current required in driving the gate capacitance of the associated MOSFET. Driver circuits offers additional functions which includes isolating the control circuit and the power circuit, detecting malfunctions, storing and reporting failures to the control system, serving a precaution against failure.

Fig. 8 shows the circuit diagram of the gate driver circuit used in this system. The IC used in this circuit is IR 2110. A diode D1, an electrolytic capacitor C3 and a ceramic capacitor C4 are connected along with the IR2110 IC. When low input signal (LIN) is high, that means 1, it turns on the MOSFET Q2 on and capacitors C3 and C4 get charged to the level on IC pin 6. When high input signal (HIN) becomes high, the capacitor C3 and C4 uses the stored charge to configure Q1 high. C3 always needs to be charged in a short period of time and it's also required to choose the large one so that it can supply the constant amount of charge to turn on MOSFET Q1. Higher capacitance is also prerequisite for higher duty cycle. The capacitance discharges by using the diode D2 and D3. Use of these diode helps to control the on off time quickly. The resistor R1 and R2 maintain the current limit on the gate of the MOSFET [21].
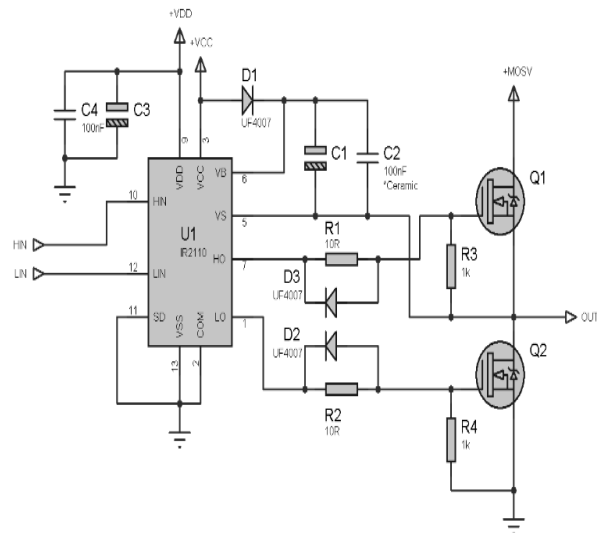

Fig. 8. Circuit diagram of the gate driver

VI. SIMULATION OF COMPLETE DESIGN

MATLAB/Simulink has been used to simulate the proposed model and the simulations have been done in two parts. In the first part fig. 9 (a) dc-dc boost converter has been simulated with PV array. The system comprises of a boost converter along with a PID controller which is inter linked with the inverter as a sub system. Here, the PID controller acts as s system to fix

the output from the boost converter to a certain level before being fed to the inverter. In the second part fig. 9 (b) the dc-dc boost converter works as the input of the inverter which is then connected to the grid. The inverter is designed using multilevel inverter topology where two separate inverters has been cascaded. The inverter is interconnected to a gate driver circuit which is used to turn on the gates of the IGBT's used in the inverter. In this particular design, 5 parallel strings are used and 3 solar modules are connected in series per string. Throughout the simulation, the solar irradiance and temperature has been kept constant at 1000 W/m^2

and 25°C respectively. As the command voltage of PID controller is set to 350V hence the controller generates the required duty cycle for the IGBT to keep the voltage constant at 350V. A DC link capacitor of 100µF has been used to smooth the output voltage of boost converter. The inverter is designed to deliver an output voltage of 400V (3 phase) with 50Hz frequency so that it can be connected directly to the grid supply of a household. The purpose of the unity transform ratio Δ-Y connected transformer used in fig. 9 is to provide only the neutral connection for the system.
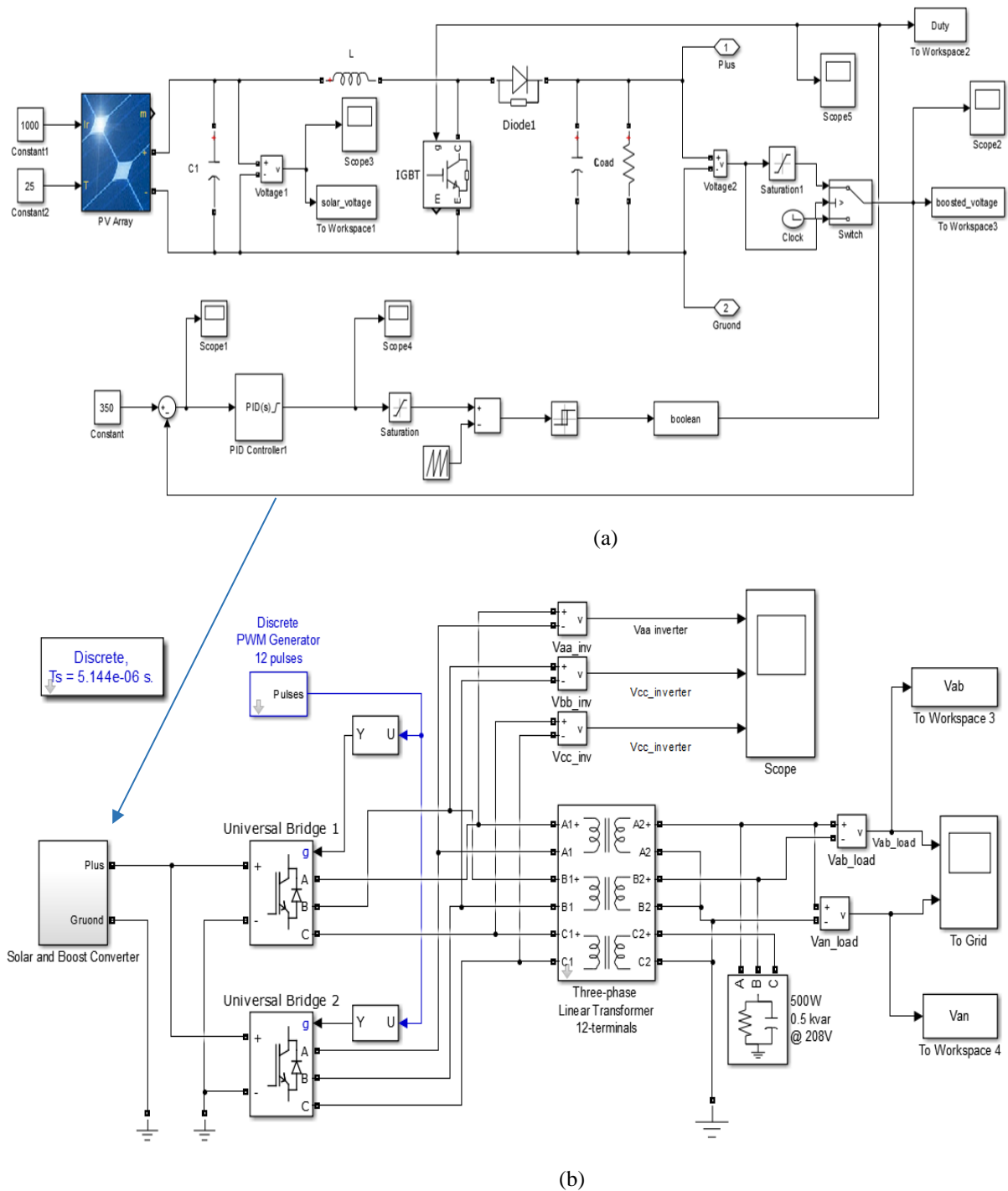

(a)

(b)

Fig. 9. SIMULINK models of (a) PV array with boost converter, (b) inverter with sub-system

VII. SIMULATION RESULTS

Outputs are obtained for PV array, boost converter and inverter. As shown in fig. 10, the maximum output that PV array can provide is 110V. Fig. 11 shows the output of boost converter. As the command voltage of PID controller has been set to 350V hence the output of boost converter has been fixed at 350V regardless of the output of PV array.
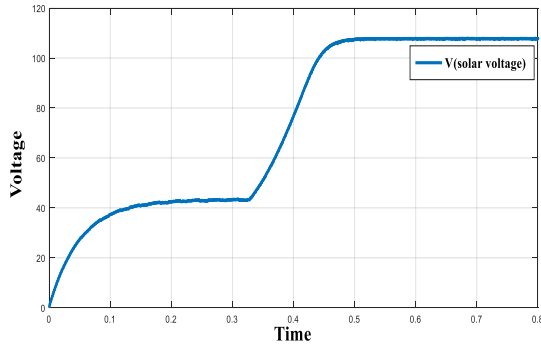
Fig. 10. Output voltage of PV array

Here, the output of the PV array varies in accordance to the availability of the solar irradiance. This does not have any impact on the output of the boost converter as the PID controller changes its duty cycle automatically to fix the output voltage from the converter to a constant level.
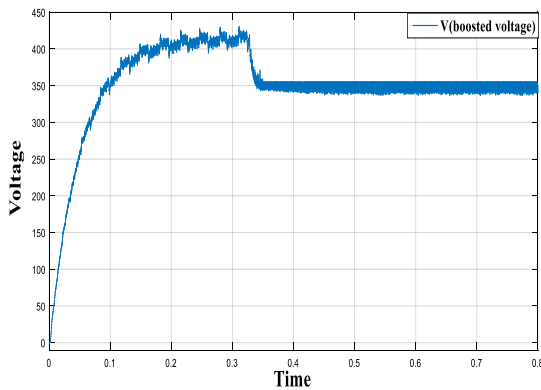
Fig. 11. Output voltage from the boost converter.

The retrieved voltage from the boost converter is always fixed to 350V for this designed system. This voltage is then fed to the inverter. The PWM pulses of the inverter has been designed in such a way so that it generates a voltage of 400V (3 phase, line to line) with 50 Hz frequency. Hence the line to neutral voltage is 220V. Fig. 12 and fig. 13 represent the line to line and line to neutral voltage of designed inverter respectively.
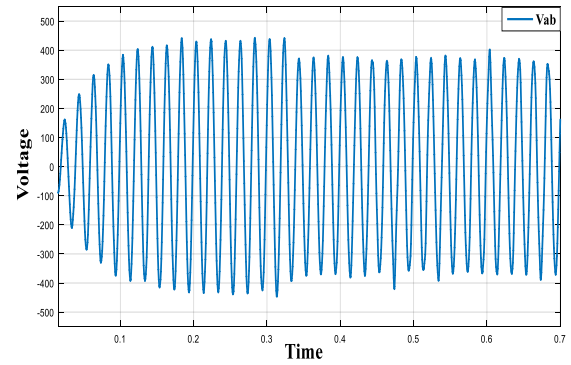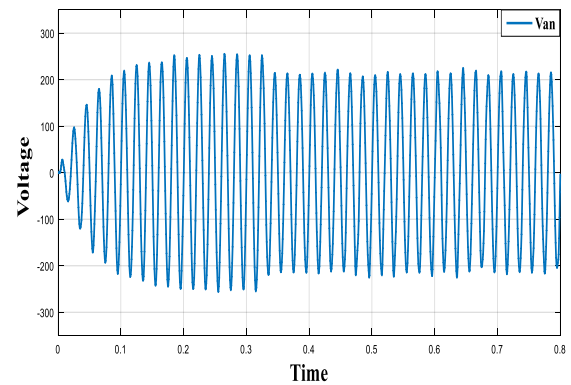
Fig. 12. Line to line at the output of inverter.

Fig. 13. Line to neutral voltage from the inverter.

A 500W and 0.5kvar wye connected balanced load has been connected with the inverter and the three phase current consumed by the load is shown in fig. 14.
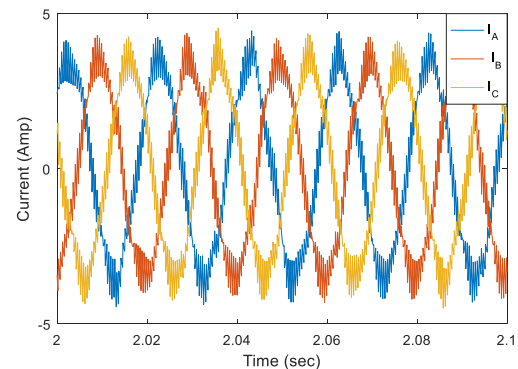
Fig. 14. Three phase current supplied by the inverter.

As no filter is used at the output of the inverter hence from fig. 14 it can be seen that it contains a lot of harmonics. Fig. 15 shows the magnitude response of current for phase A. It reveals that because of high frequency switching of the inverter, there are a significant amount of high frequency harmonics present in the inverter current, especially from 2000Hz to 2300Hz range.
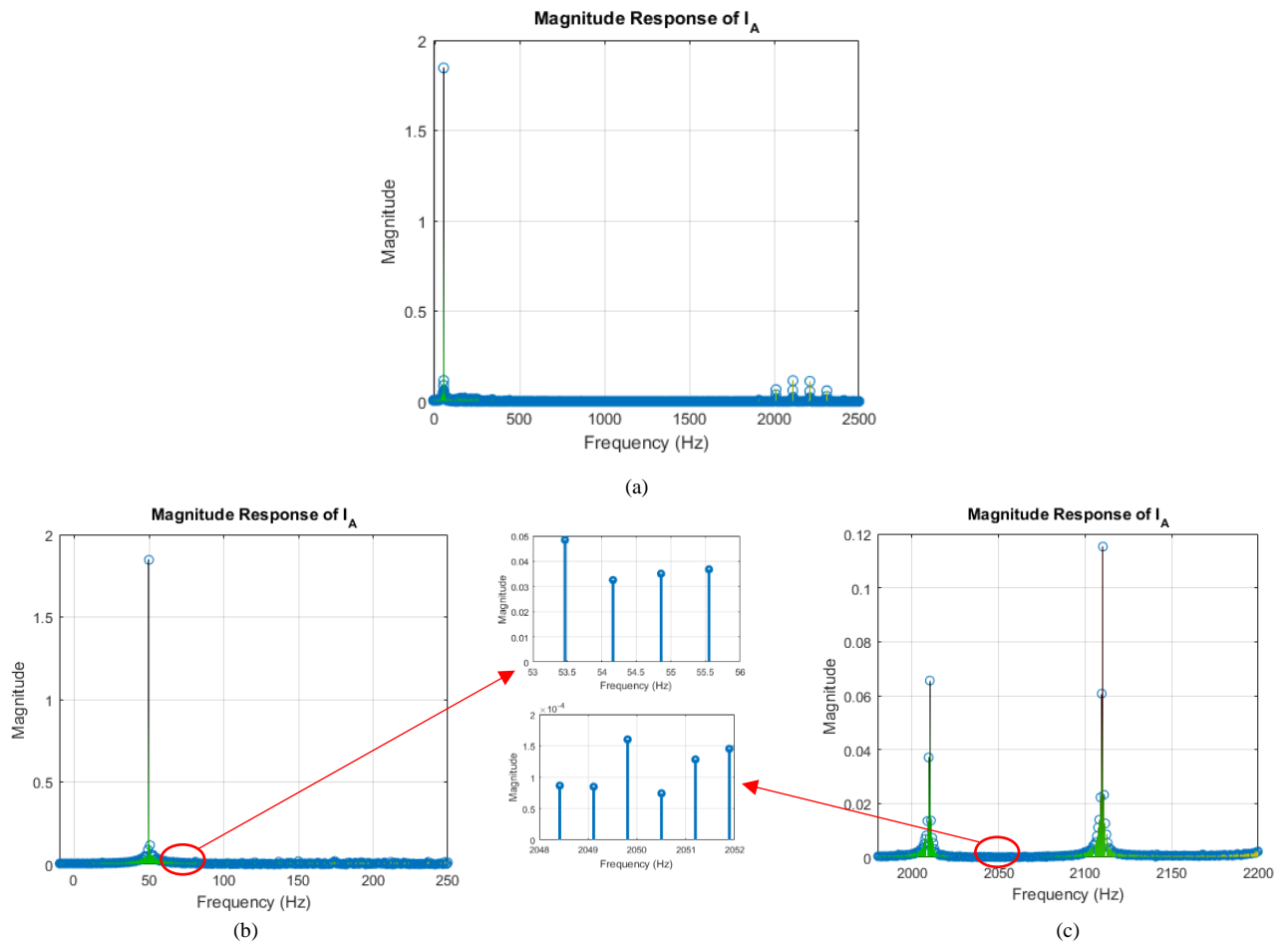
(a)

(b)   (c)

Fig. 15. Magnitude Response of current for phase A (a) From -10Hz to 2500Hz (b) -10Hz to 250Hz (c) 1980Hz to 2200Hz

VIII. PROTOTYPE IMPLEMENTATION AND RESULTS

A small prototype has been implemented for a small scale voltage. A PID controller, a gate driver circuit and an inverter circuit has been implemented as shown in fig. 16, fig. 17 and fig. 18 respectively.

The PID controller have been implemented in a PCB using a variable pot for the tuning. Using an Arduino the PID controller algorithm has been developed. The fig. 16 shows the implementation.
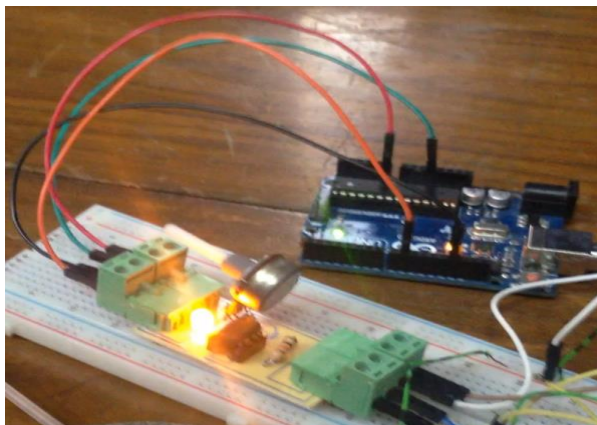

Fig. 16. The setup showing the PID controller

For proposed prototype model three gate drivers have been implemented to generate 6 sets of output. Each of these outputs has been used as gating pulse in the six set

of IGBT's in the inverter circuit. This driver circuits also works as isolation for the inverter circuit. The gate driver has been implemented in a PCB board as shown in the fig. 17.
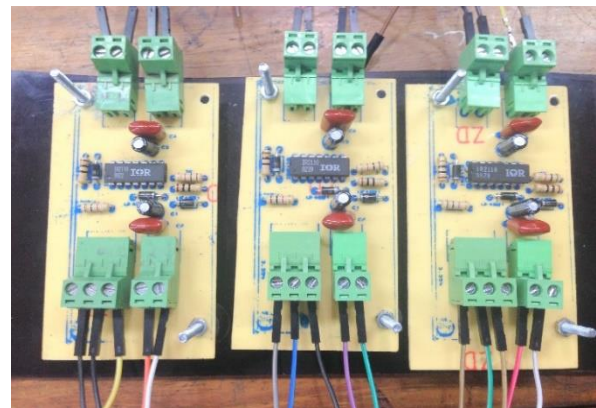

Fig. 17. The implementation of gate driver circuit

Fig. 18 shows the complete implemented system with the gate driver and the inverter synchronized. Here Arduino Uno have been used as the controller which is shown in the simulation part.
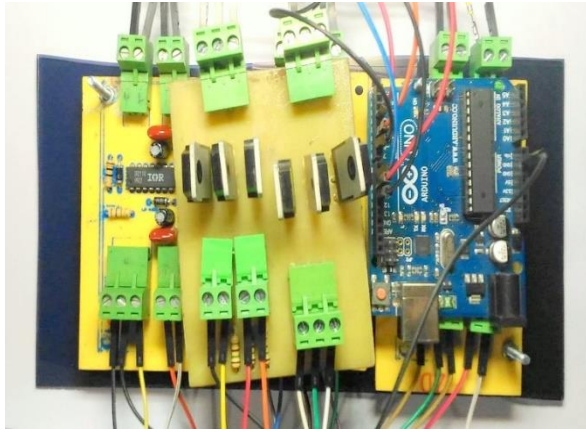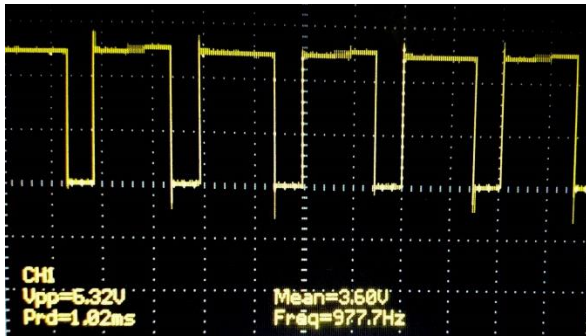
Fig. 18. Inverter circuit with the overall system

Fig. 19. Output from the PID controller

The output from the PID controller is limited to ±5 volt as pulse was generated by the means of Arduino Uno. A Saw-tooth wave was generated using a function generator and the output was fed to a comparator circuit along with the output from the Arduino. The output from the comparator circuit was varied using a potentiometer as shown in the above fig. 16.
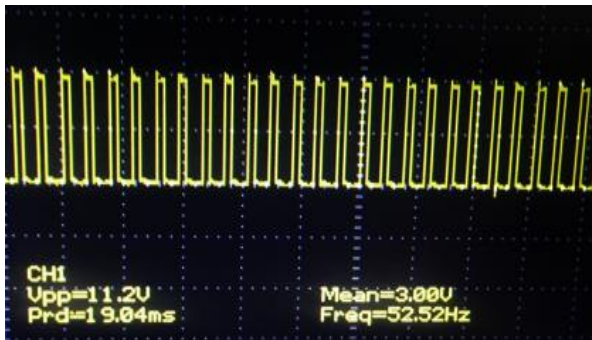

Fig. 20. Output result of gate driver circuit

The output shown in fig. 20 was the output obtained from the implemented gate driver circuit. Usually when a pulse of an amplitude of 5 volt is fed into a gate driver circuit, a 12 volt amplitude pulse is expected in return. The obtained result shows a successful output of the implemented circuit.
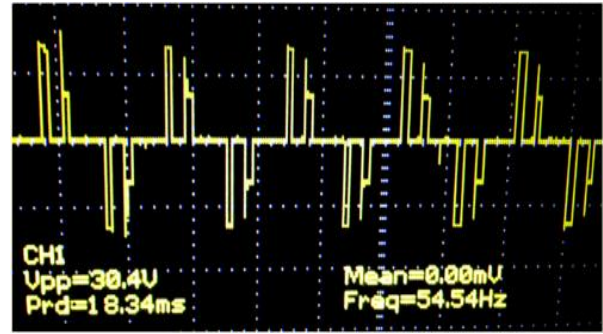

Fig. 21. Line to neutral voltage from the inverter

Fig. 21 shows the output waveform from the inverter. The obtained wave shape is not totally sinusoidal because in the implemented prototype two inverters has not been cascaded. Increasing the number of levels will smoothen up the wave shape.

IX. COMPARISON OF TRANSFORMER LESS AND TRANSFORMER BASE INVERTER TECHNOLOGY

Transformer-less inverter technology has several advantages over conventional transformer base inverter. Eliminating the transformer brings several advantages like it makes the inverter much lighter, compact, more affordable also reduces the cost of the inverter. 30 different inverters were compared by Dhivya, Santoshamma [22] of which seven were transformer-less and rest of them are transformer-base inverter. Price and efficiency of the proposed transformer less system has been calculated and compared with the transformer-base system which is summarized in table 1. Efficiency is calculated by dividing measured output power by input power which results 95.9% for the implemented system.

Table 1: Comparison of inverters for grid tied PV system

Design Type	Efficiency (%)	Price ($/W)
With Transformer [10]	93.1	1.95
Proposed Transformer less	95.9	1.47

So, it is clear from above comparison that transformer-less inverter is nearly cheaper than conventional transformer base inverter. However, having several advantages safety issue is the major concern for transformer-less inverter. Transformer-less inverter lacks electrical isolation between DC and AC part of the system. Transformer-less inverter may also develop quite stronger electromagnetic field than transformer base inverter. In order to eliminate these issues, in this design, a unity gain transformer is used. The cost of a unity gain transformer is much more lesser than the conventional step up or step down transformer. This unity gain transformer will solve the insolation problem and make earth fault detection easier as a neutral path is obligatory for the detection of earth fault.

X. CONCLUSION

This paper represents the design, simulation and practical results of a grid-tie multilevel inverter for PV application. Although the prototype is designed in small scale but after analysis it can be seen that the simulation results resembles the practical results and

fulfill the objectives of the project. In this proposed design, the duty cycle for the boost converter will be varied automatically with the variation of the output voltage of PV arrays. Hence it is possible to keep the voltage constant as incident solar irradiance varies throughout the day. Finally, as the generated power is directly supplied to the grid hence it is possible to avoid the capital and maintenance cost of battery pack. Like every other projects, there are also few shortcomings of this project. The inverter output was directly connected to the grid with no filter circuit between the inverters output and the grid. A filter circuit could provide a much better waveform to the grid by eliminating the harmonics from the inverter output. In the designed prototype, constant DC source was used instead of PV array. If a PV array were used, it might affect the output waveform of the inverter. The stated shortcomings can be considered as a part of future work.

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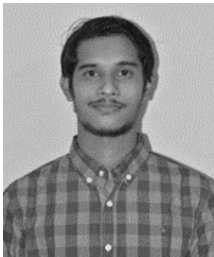
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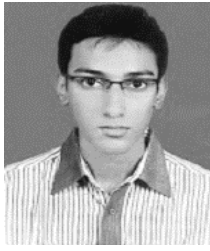
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