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Design and Analysis of Logic Gates using GaN based Double Gate MOSFET (DG-MOS)

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***Abstract*— The double gate MOSFET, where two gates are fabricated along the length of the channel one after another. Design of logic gates is one of the most eminent application of Double Gate MOSFET. Gallium nitride (GaN) based metal-oxide semiconductor field-effect transistors (MOSFETs) are shown to be promising for digital logic applications. This paper describes the design and analysis of different types of logic gates using GaN based DG-MOSFET. The gate length (LG) is kept constant at 10.6 nm. The gate voltage varies from 0 to 1 V for the device switching from turn OFF to turn ON-state. For the device with HfO_2 as gate oxide, the ON-state current (I_{ON}) and OFF-state current (I_{OFF}) are found 8.11×10^{-3} and 6.38605×10^{-9}A/μm respectively. The leakage current is low for the device with HfO_2 as compared to that for the device with ZrO_2. The subthreshold swing (SS) is 68.7408 mV/dec for the device with HfO_2.**

Keywords*— GaN, Double Gate MOSFET, nanoscale, logic applications;

I. INTRODUCTION

MOSFET is a very promising candidate for logic applications. For future logic devices we need to shrink up the devices in nanoscale regime. Conventional Si-based transistors are scaled-down in size according to Moore's law [1]. The primary goal of scaling of MOSFET is to achieve the speed and efficiency but it fails in the area of leakage [2]. A new material for the devices in nanoscale regime is needed to meet the future demand. Gallium Nitride-based semiconductors have been spectacular due to their highly attractive vital properties. The superior properties of the Gallium Nitride based materials are; it has lower effective mass for electrons, large band gap, high mobility and high saturation velocity [3]. Thus, Gallium Nitride is a highly potential material for the fabrication of high-speed, high performance FETs [4]. GaN as a channel material has already been considered for regular channel devices and proved its superiority. But for nanoscale devices, it is not premeditated in detail.

Scaling down the MOS-transistors is one of the major issues nowadays for the semiconductor industries. DG-MOSFETs have good electrostatic gate control over the channel in sub-10nm regime [5]. Though Si based DG-MOSFETs reduces the SCEs [6] have limitations such as low mobility, high gate leakage current, and high delay time. To overcome the Short channel effects of Gallium Nitride based DG-MOSFETs the underlap length is extended in both source and drain sides that increases the effective channel length, thereby increasing the series resistance in underlap regions. Moreover, using underlap length, in sub-threshold region it reduces gate edge direct tunneling leakage and gate sidewall fringe capacitance due to increasing of effective channel length that ensures better performance. Therefore, it is immense important to design and analysis of logic switching devices. The DG-MOSFETs provide excellent immunity to SCEs and better scalability [7]. As a result, both DIBL and subthreshold slope (SS) values are improved [8-10] means reduction of SCEs.

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Due to better electrostatic control over the channel, double gate (DG)-MOSFETs have shown superior performance in comparison with the conventional single gate MOSFETs [11].

The DG-MOSFETs show excellent immunity to SCEs and better scalability [12]. As a result, both DIBL and subthreshold slope (SS) values are improved [13-15].

In this paper, the effect of GaN based Double Gate MOSFET has been described with Gate Length 10.6nm also the digital application of GaN based Double Gate MOSFET.

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II. Device Structure

Fig. 1 shows the basic structure of double gate MOSFET. As it is mentioned earlier, both gates are fabricated along the length of the channel. For that, both gates affect the current flowing between source and drain.

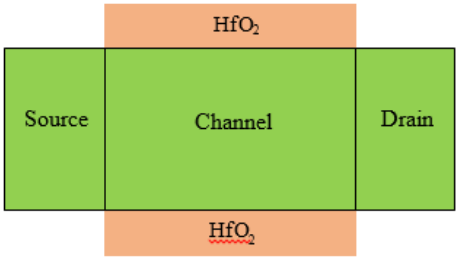
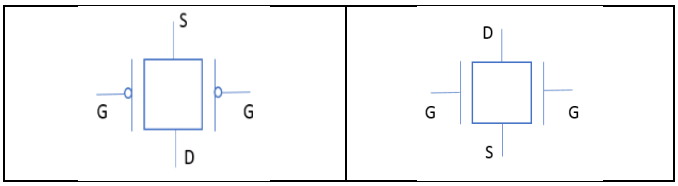


Fig. 1. Basic Structure of DG-MOSFET.

In case of effect, the operation of double gate MOSFETs can be considered as the operation of two MOSFETs which are in series [16]. There are two types of Double Gate MOSFETs, i) p-type Double Gate MOSFET ii) n-type Double Gate MOSFET.



(i) (ii)

Fig. 2. Types of DG-MOSFET i) p-type ii) n-type

Table I shows the parameters used in to design the GaN based Double Gate MOSFET.

TABLE I. Parameters Used in the Simulation of the Device Structure

Parameters	Values
Gate Length	10.6nm
Source and Drain Length	5nm
Effective Oxide Thickness	0.59nm
Thickness of Di-Electric Material [HfO_2]	3.33nm
Body Thickness	3.4nm
V_{DD}	0.75V
Channel Dopping	$1X10^{17}$ cm^{-3}
Body Dopping	$1X10^{20}$ cm^{-3}

All structure is simulated under the consideration of GaN effective mass of electron $me^*=0.18\ m_0$ using SILVACO Atlas TCAD tool.

III. Results

Fig. 3 shows the On state and Fig. 4. Shows the Off state of GaN based Double Gate MOSFET. Where Electron concentration have been showed. In Fig. 3 the electron concentration is high due to on-state. But in off-state it is poor. The dc-output characteristics of GaN-based DG-MOSFET have been shown in Fig. 5 for L_G = 10.6 nm. The device exhibits the well pinch-off condition at V_{GS} = 0 V and a high ON-state current, I_{ON} of 8.11e-3 mA/µm at V_{GS} = 1 V. Therefore, OFF-state and ON-state is considered as V_{GS} = 0 V and V_{GS} = 1 V, respectively. In Fig. 6 the transfer characteristic of the GaN-based MOSFEET. The highest value of I_{ON}=8.11e-3 A/µm is achieved for gate length, L_G=10.6nm. For each L_G with fixed V_{DS}=0.75 V, it is clear that in the linear region the drain current (I_D) is proportional to the conductivity of channel and in the saturation region I_D is proportional to the carrier density and injection velocity.

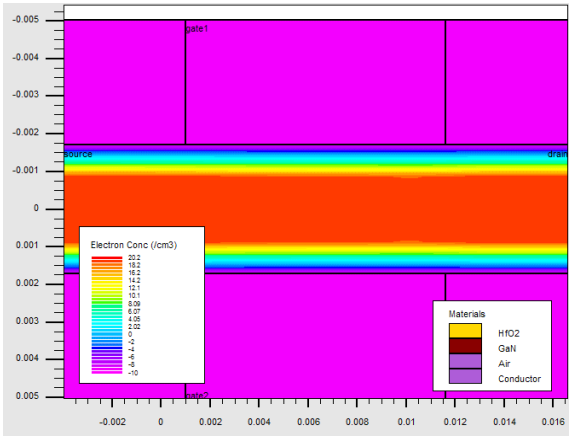


Fig. 3. On state of GaN based Double Gate MOSFET

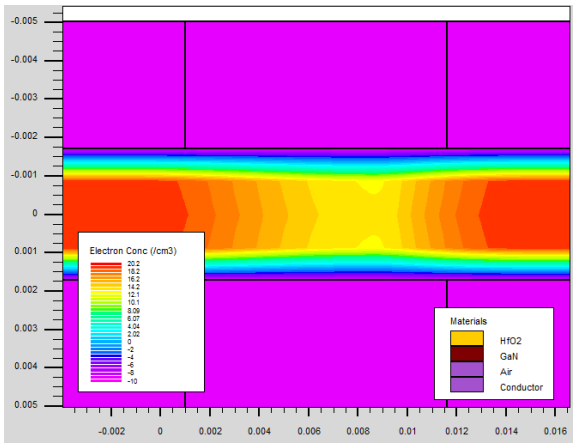


Fig. 4. Off state of GaN based Double Gate MOSFET

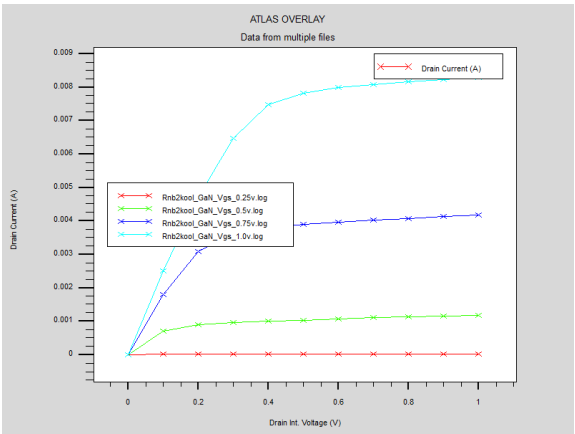


Fig. 5. O/P characteristics of GaN based DG-MOSFET.

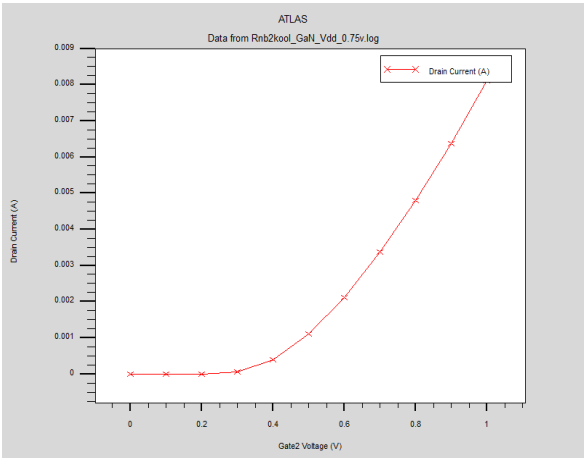


Fig. 6. Transfer characteristics of GaN based DG-MOSFET.

The following values have been found from the simulations.

TABLE II. VALUES FOUND FROM SILVACO ATLAS TCAD TOOL

Channel Length	**10.6nm**
I_{on}	8.11×10^{-3}
I_{off}	6.38605×10^{-9}
I_{on}/I_{off}	1.27042×10^{6}
DIBL	0.0634143
Threshold Voltage at V_{DS}=0.2V	0.353521
Threshold Voltage at V_{DS}=0.75V	0.156415
Subthreshold Slope	0.0687408
Linear Gain(Beta)	0.023085
Mobility (Theta)	0.948668
Body effect (Gamma)	-0.0905337
I_{dsmax}	0.00811296
Leakage Current	0.00811296

Table II shows the values found from Silvaco TCAD Tool by extraction method. The founded parameters are compared with the model parameters of HSPICE. Table III shows the HSPICE model parameters measured from the simulation of Silvaco TCAD Tool.

TABLE III. HSPICE MODEL PARAMETERS FOUND FROM SILVACO TCAD TOOL

Parameter Name	**Value**
LEVEL	49
VERSION	3.11
PARAMCHK	0
CAPMOD	2
MOBMOD	1
ELM	5
TOX	3.33E-009
XJ	0.0015774
KETA	-0.047
VOFF	0.08
XT	1.55E-007
VTH0	-0.329592
NCH	1E17
NSUB	1E20
NLX	1.74E-7
GAMMA1	1.28248
GAMMA2	1.28248
K1	1.28248
W0	5E-009
DVT1W	5.3E+006
ETA0	-0.89831
ETAB	-0.89831
U0	2.5113
VSAT	0.25
DELTA	0.01
CF	1.05449E-10
TNOM	298.15
KT1	-0.0905337
KT2	-0.0905337
JS	0.00196496

A. Not Gate With N-Type Double Gate Mosfet With Resistive Load Only

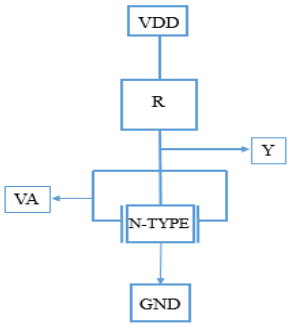


Fig. 7. Basic circuits of N-Type GaN based DG-MOSFET NOT GATE with Resistive load

Fig 7 shows the basic circuit of NOT gate with Resistance as load. Here the gates of the device is symmetric. Here the resistance is connected between V_{DD} and drain terminal of N-type DG-MOSFET. Also gate terminal is connected with V_A which is pulse. The output is measured from drain terminal. Source is connected to the ground. Again assuming that V_{DD} is

logic 1 and Ground is logic 0. If we give 0 in pulse V_A, N-type DG-MOSFET will be in off condition and behave like an open circuit. And the output will be logic 1 with some drop due to resistance. If we give 1 in pulse V_A, N-type DG-MOSFET will be in on condition. And there is On Resistance. By applying voltage divider rule, the measured output will be approximately 0.

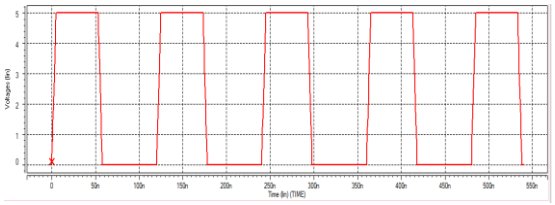


Fig. 8. Input Pulse V_A

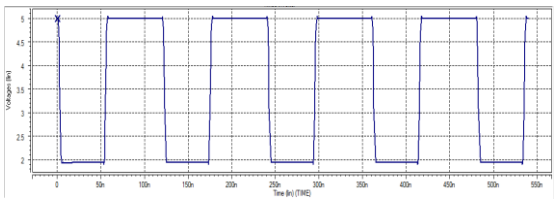


Fig. 9. Output

Fig. 8 represents the input pulse V_A that is input pulse; and Fig. 9 represents its output. When V_A is high output is low and when VA is low output is high.

B. Not Gate Using N-Type Double Gate Mosfet With N-Type Load

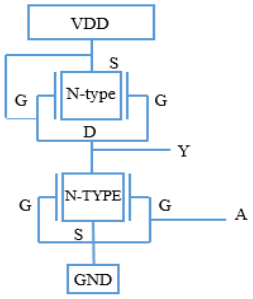


Fig. 10. Basic circuits of N-Type GaN based DG-MOSFET NOT GATE with N-type load

Fig. 10 shows the basic circuit of NOT gate with N-type load. Here the gates of the device is symmetric. Here the N-type load is connected between V_{DD} and drain terminal of N-type DG-MOSFET. Also gate terminal is connected with A which is pulse. The output is measured from drain terminal. Source is connected to the ground. Again assuming that V_{DD} is logic 1 and Ground is logic 0. If we give 0 in pulse A, N-type DG-MOSFET will be in off condition and behave like an open circuit. And the output will be logic 1 with some drop due to resistance. If we give 1 in pulse V_A, N-type DG-MOSFET will be in on condition. And there is must be internal Resistance drop. By applying voltage divider rule, the measured output will be approximately 0. Figure 11 shows the Input pulse of A and 12 shows the output. As it is has been seeing from the figure that when the input is low output is high and input is low output is high.

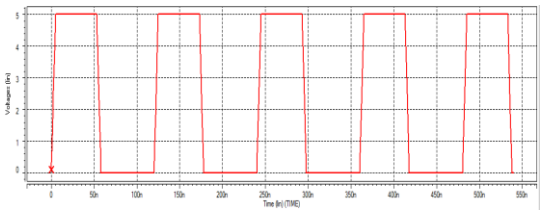


Fig. 11. Input Pulse A

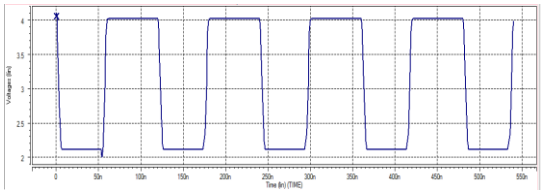


Fig. 12. Output Y

C. Not Gate Using P-Type Double Gate Mosfet

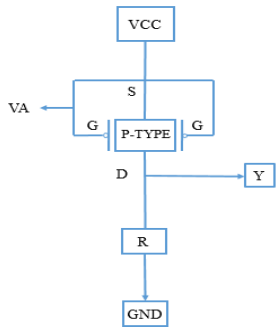


Fig. 13. Basic circuits of P-Type GaN based DG-MOSFET NOT GATE

Fig. 13 shows the basic circuit of P-type DG-MOSFET NOT gate. The gate terminals are symmetric and connected with Pulse V_A. V_{DD} is connected with source terminal and Resistor is placed in between Drain and ground. As we know P-type turns on at low voltage. Assuming that V_{DD} is logic 1 and Ground is logic 0. Theoretically, if we give 0 in pulse then p-type DG-MOSFET turns on and act like short circuit and output will be logic 1 or V_{DD}. If 1 is given it will show the output is zero. But due to resistance there must be drop of voltage because current will flow through resistance.

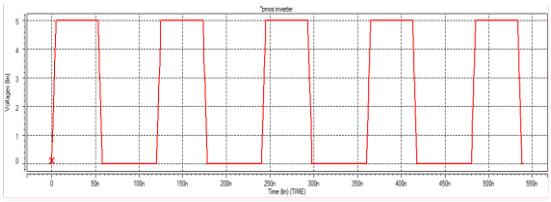


Fig. 14. Input Pulse V_A

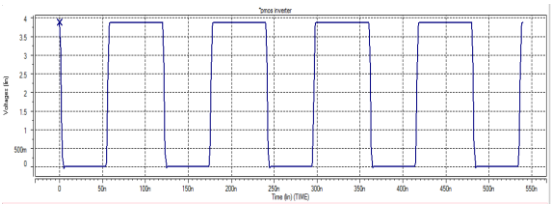


Fig. 15. Output Y

D. CMOS NAND Gate Using Double Gate MOSFET

The schematic diagram of a 2-input CMOS NAND gate using GaN based DG-MOSFET is shown in Fig. 16.

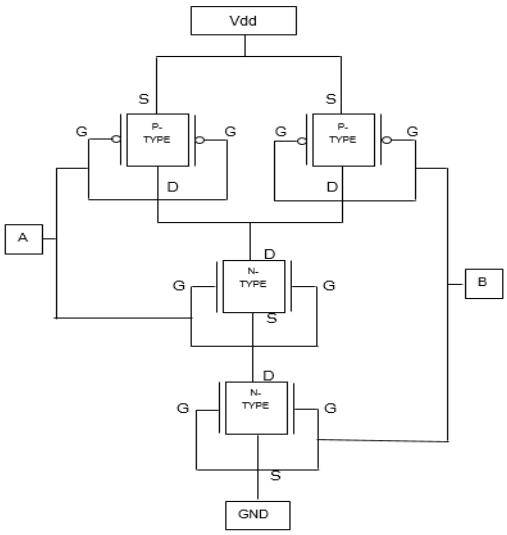


Fig. 16. Basic circuits of GaN based DG-MOSFET CMOS NAND Gate

Here, N-type transistors are connected in series while the P-type transistors are connected in parallel. Table IV shows the input output condition of CMOS NAND gate using Double gate MOSFET. The switch equivalent is shown for the case where Input A is HI and Input B is LO.

TABLE IV. INPUT OUTPUT OF CMOS NAND

IN A	IN B	T1	T2	T3	T4	O/P
LO	LO	OFF	ON	OFF	ON	HI
LO	HI	OFF	ON	ON	OFF	HI
HI	LO	ON	OFF	OFF	ON	HI
HI	HI	ON	OFF	ON	OFF	LO

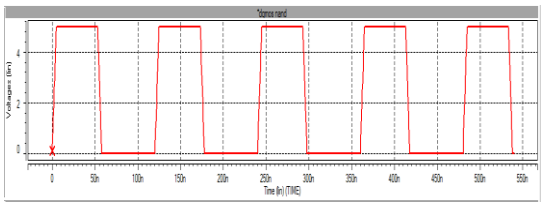


Fig. 17. Input Pulse V_A

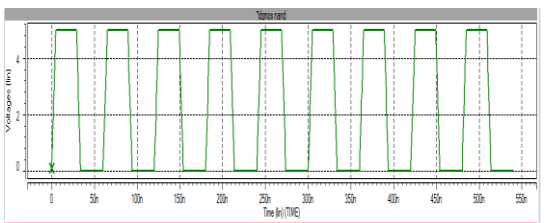


Fig. 18. Input Pulse V_B

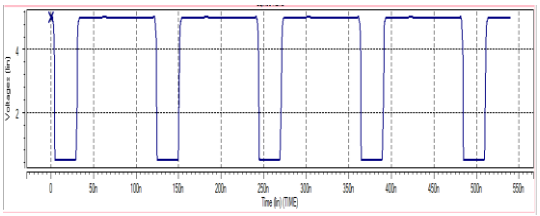


Fig. 19. Output

IV. CONCLUSION

GaN-based DG-MOSFETs have been designed according to the ITRS (2013) requirements for HP devices. Key device matrices such as ION, SS, and DIBL have been evaluated and the results have been compared with Si-based DG MOSFETs. From the results it can can be determined that using GaN-based DG-MOSFETs both leakage current and the SCEs can be reduced and better control over the channel can be obtained. Therefore, it can be concluded that GaN-based DG-MOSFETs are very promising candidate for manufacturing high speed, high performance (HP) devices.

Compared to silicon, GaN's electrons make it capable of conducting many thousand times more power than silicon, giving it applications. It has been shown in previous research that GaN has a higher critical electric field strength than silicon. Its higher electron mobility enables a GaN device to have a smaller size for a given on-resistance and breakdown voltage than a silicon semiconductor. Compared to silicon devices, this also allows devices to be physically smaller and their electrical terminals closer together for a given breakdown voltage requirement.

Because of excellent transport properties, high performance GaN material is a promising candidate of replacing Si from the channel. GaN as a channel material has already been considered for regular channel devices and proved its superiority. But for nanoscale devices, it is not premeditated in detail. The performance of GaN-based nanoscale MOSFET for gate length less than 12nm and simulated the performance of the device by NEGF method.

In this paper, different types of digital logic gates had been designed and analyzed using GaN based double gate MOSFET has been used. In some cases, there is voltage drop due to the on resistance of the MOSFET. GaN based DG MOSFETs show better short-channel behavior, lower leakage current and higher drive current than other MOSFET structures.

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