Published in AJSE, Vol:20, Issue: 3
Received on 4th May 2021
Revised on 18th September 2021
Accepted on 21st September 2021

AIUB JOURNAL OF SCIENCE AND ENGINEERING
ISSN: 1608 – 3679 (print) 2520 – 4890 (Online)

Linearization of High frequency Class E Feedback Amplifier using Negative Impedance Method

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***Abstract*— This work represents a novel method of linearization of Switch Mode Power Amplifier (SMPA). For this purpose, class E SMPA was designed and analyzed both before and after applying a linearization technique known as the Negative Impedance method. One of the major characteristics of a standard SMPA is that they have higher efficiency than their linear counterpart but on the other hand they show highly nonlinear characteristics. The motivation behind this work is to harness this highly efficient amplifier and make it linear which can be very useful for various applications in RF communication fields. All the schematics and simulations that are presented in this paper were performed using the Cadence Virtuoso environment using the "Spectre" simulator tool. For active components, 280nm process technology was used under "gpdk90" pdk which is based on BSIM3v3 model. The gpdk90 package includes devices ranging from 100nm to 280nm processes for different voltage levels. The 280nm process was chosen as it supports a maximum of 2.5V of supply. The Circuit was designed to run at 2GHz with 2.5 V supply voltage. A mathematical model is also presented using data found from the analysis, with the help of MATLAB. Linearity was measured using Input referred Intercept Point of 3rd order frequency (IIP3), which was improved from 3.7dBm to 17.86dBm with 57% percent efficiency providing an output power of 15.78dBm.**

Index Terms— *SMPA, Class E amplifier, Linearity, IIP3, PAE, Schmitt Trigger*

I. Introduction

At present, the 4th industrial revolution is becoming more and more apparent. The 4th industrial revolution enables all the modern technology used in every sphere to combine into a single entity where the technologies can communicate to each other for better functioning of the device itself as well as for the whole system. Thus, machine-to-machine wireless communication will be on the rise. So, it is crucial to develop circuit designs to improve wireless RF communication. One of the most used circuits in the RF field is a power amplifier (PA). One can find at least one PA in every transmitter or receiver block in the communication system. They are also used in repeaters to increase the signal strength in long transmission mediums. There are two basic types of PA, one the linear PA other one is Switch Mode PA. The basic difference between them is that linear PA has active devices working in the saturation region, unlike SMPA where the active device works only as a switch. This makes the SMPA advantageous over its linear counterpart in terms of efficiency but SMPA suffers from nonlinear behavior. Hence special care needs to be taken to improve linearity. There are many linearization techniques available. The most prominent ones are feedback, feedforward, cross cancellation, Analog pre-distortion, digital pre-distortion, negative impedance method, etc. In this work, a Class E SMPA was designed running at 2GHz with 2.5 V supply and analyzed utilizing the negative impedance method, which is an extended version of the previous work cited in [5]. The contribution of this work is the concept of applying the negative impedance method in switch-mode power amplifiers such as Class E amplifiers and analyze their behavior. The simulation analysis was done both before and after applying the linearization technique. All the simulation was done using Cadence Virtuoso utilizing "Spectre" simulator tool. Later on, a mathematical model was introduced which is generated from Spectre and modeled using MATLAB. The active device for this work is from "gpdk90" Process Design Kit (PDK) consisting MOSFETs in 280nm process technology. The gpdk90 package includes devices ranging from 100nm to 280nm processes for different voltage levels. The 280nm process was chosen as it supports a maximum of 2.5V of supply.

This paper was submitted to AIUB Journal of Science and Engineering (AJSE) on May 4th , 2021. Special thanks to AJSE committee for accepting this work and for adding value to this work by giving constructive reviews.

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II. EARLIER RESEARCH

One of the earliest researches on class E SMPA was carried out by N.O.Sokal et al [1] back in 1970 where a basic understanding of SMPA was presented mentioning design methodologies and compared different types of PAs. The following table shows a comparison of PA in terms of max power delivered and maximum frequency.

TABLE I Comparison among different types of PA

Class	Pmax (W)	Efficiency (%)	Comments
A	0.125	50	360º conduction angle
B	0.125	78.5	180º conduction angle
C	0.0981	89.6	120.6º conduction angle
	0	100	0º conduction angle
D	0.318	100	Uses two devices
E	0.0981	100	Optimum 50% duty cycle
F	0.159	100	Infinite number of resonators
S	0.125	100	AC coupled

The values that are presented in table 1 are found from [1] and all the values are taken considering ideal conditions. A more intuitive as well as calculative approach was given in a book in [2] by Hella et al. where a class E amplifier is designed for personal area networks. Functional block diagram for class E SMPA can be found in both [1] and [2], where the SMPA is divided into three blocks namely, the driver stage, the active switch, and the load network. On the other hand, a slightly different approach was taken by R.Kubowicz in [3], where a class E amplifier was imagined as an RLC tank circuit. According N.O.Sokal and Hella et al., the driver stage must produce square pulses of 50 % duty cycle to provide an equal amount of time to charge and discharge the energy stored in the inductor and capacitor of the resonator. On the other hand, A. Mediano et al in [4] presented a circuit design of a class E amplifier that can operate at any duty cycle with the help of very large shunt capacitance across the switch. Again, a unique approach was shown in [5] by M.S. Sikder where a Schmitt trigger is utilized to make 50 % duty cycle square pulses to drive a class E amplifier making the design cost-effective in terms of low area. Among the earliest research on linearization technique feedforward technique is a prominent one done by Bennett et al in [6]. A bit more advanced designs were described by T. Rahkonen et al in [7] where an analog polynomial pre-distortion circuit utilizing the gilbert cell to reduce the spectral widening. Furthermore, Chi – Tsan Chen et al in [8] described an approach involving a digital envelop predistorter to linearize a class E power amplifier. Moreover, P Sampath et al in [9], designed an analog pre-distortion with the help of the square law method. In this work, another modern approach was utilized which known negative impedance method developed by M.T.Ali et al shown from [10] to [12] where an adjustment current is introduced at the input side of a differential amplifier which helps to increase its linearity. The novelty of this work is the application of this method on a highly nonlinear class E switch-mode power amplifier and observe its linearity as well as other performance parameters. All the simulation results that are shown in this paper are done in the cadence virtuoso environment using "Spectre" simulator [13]. The active devices are 280nm CMOS process of "gpdk90" pdk using "BSIM3v3" device model [14]. In the end, a class E amplifier was achieved running at 2GHz delivering 15.78dBm of power at the output with IIP3 of 17.86dBm

III. SCHEMATIC DESIGN

A. *Design Conditions*

In [1] and [2] the authors have clearly described design methodology and key concepts for SMPA, especially on Class E Power Amplifier. Some of the important considerations and conditions are shown below,

- At the moment of turning on, there should be no voltage drop across the active switch and the voltage slope should be zero as well.
- The output of the driver should produce square wave pulses of 50% duty cycle.
- There is a tradeoff for increased device sizes and turn-on resistance. With increased width, the on-resistance will drop but it will increase its parasitic capacitance which impacts the resonant frequency.

B. *Circuit Description*

R.Kubowicz has shown his work given in [2] describing the Class E Amplifier as RLC parallel circuit. The designed functional circuit using ideal components is represented in figure 1.

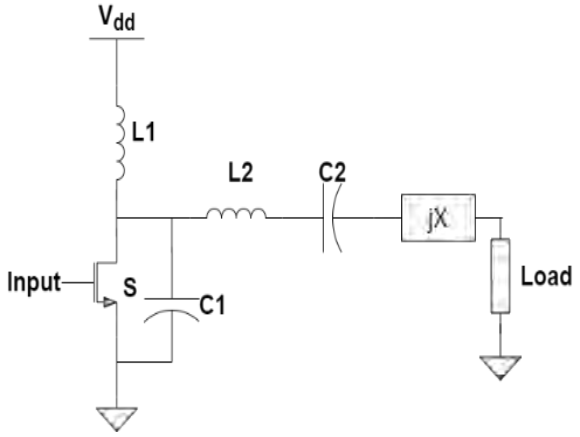


Fig. 1. Functional schematic of class E amplifier [3]

In the figure, it is depicted that the device S is a MOSFET acting as a switch with choke inductance L1, and C1 is the shunt capacitance connected at the drain terminal. The input of the switch comes from the driver stage. The inductor-capacitor series circuit shown as L2 and C2 acts as a series resonant circuit with a resonant frequency of 2GHz. The inductance jX

shown in the figure fixes the phases of voltage and current at the output delivering power to the load. The values of the passive elements are shown in the following table.

TABLE II Values of the passive components

Components	Values
Choke inductor, L1	5nH
Phase correction inductor, jX	500pH
Shunt capacitor, C1	500fF
Series resonance capacitor, C2	672.17fF
Series resonance inductor, L2	2.18nH

C. *Driver Circuit design*

In this work, the driver stage was chosen to a Schmitt trigger type for which the design is found from [5] by M.S. Sikder. The design of the driver stage is shown in figure 2.

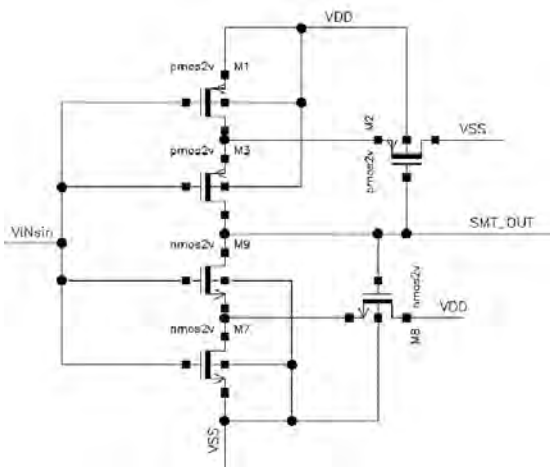
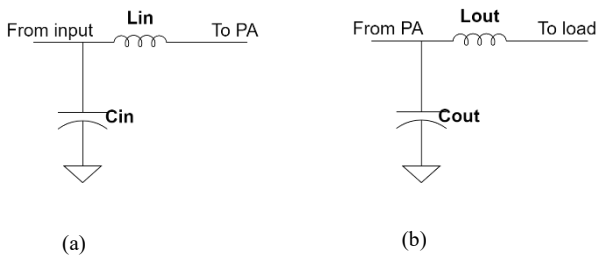


Fig. 2. Schmitt Trigger Schematic.

According to C.Zhang in [15], the Schmitt trigger gives more noise immunity as well as control over the switching threshold by adding hysteresis.

D. *Impedance Matching Network*

The load matching or impedance matching network is used to deliver maximum available power to the load. The impedance of the ports is taken to be 50ohms standard load according to [16]. Both input and output impedance was measured in simulation by pumping 1 A of current at each designated net and measured the voltage on that net. The input and output impedance was found to be 325ohms and 80ohms. The matching networks for both input and output are shown in figure 3.



(a) (b)

Fig. 3. Impedance matching network (a) input side (b) output side

The values of the inductor and capacitor for the matching network are found from the equations found in [17] and shown below.

For matching network at the input side shown in figure 3(a)

$$Q = \sqrt{\left(\frac{RL}{RS} - 1\right)} \quad (1)$$

$$Cin = \frac{Q}{\omega RL} \quad (2)$$

$$Lin = \frac{1}{\omega^2 \times C1}\left(\frac{Q^2}{Q^2+1}\right) \quad (3)$$

For matching network at the output side shown in figure 3(a)

$$Q = \sqrt{\left(\frac{RL}{RS} - 1\right)} \quad (4)$$

$$Cout = \frac{QRS}{\omega} \quad (5)$$

$$Lout = \frac{1}{\omega^2 \times C2}\left(\frac{Q^2}{Q^2+1}\right) \quad (6)$$

Here in equations (1), (2), and (3), RL and RS stand for the input resistance of the amplifier along with the driver and input port resistance respectively. On the other hand, in equation (4), (5) and (6), RL and RS is the port impedance and amplifier output impedance. Moreover, Cin and Lin are the inductor and capacitor for the input side matching network and Cout and Lout are for the output side matching network respectively. After some further tuning, the following values were found which are shown in Table II.

TABLE II Matching network element values

Elements	Name	Value
Inductor	Lin	21.72nH
	Lout	2.18nH
Capacitor	Cin	282fF
	Cout	672.17fF

E. *Circuit Operation*

The basic understanding of the class E amplifier can be found in [1] and [2], where it has been divided into three functional parts. The block diagram in figure 4 shows their functional behavior.

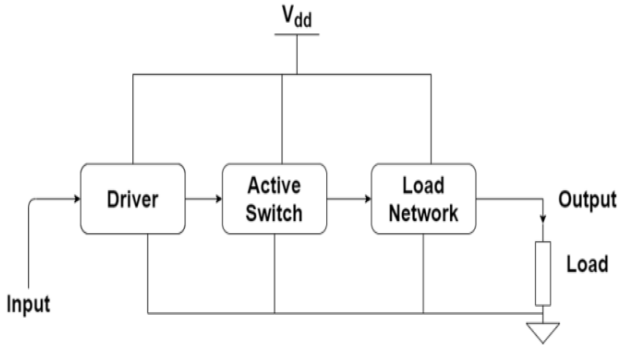


Fig. 4. conceptual block diagram class E switch-mode power amplifier.

The circuit operations can be described as RLC resonant circuit according to R Kubowicz in [3]. The equivalent circuit is presented below in fig 5.

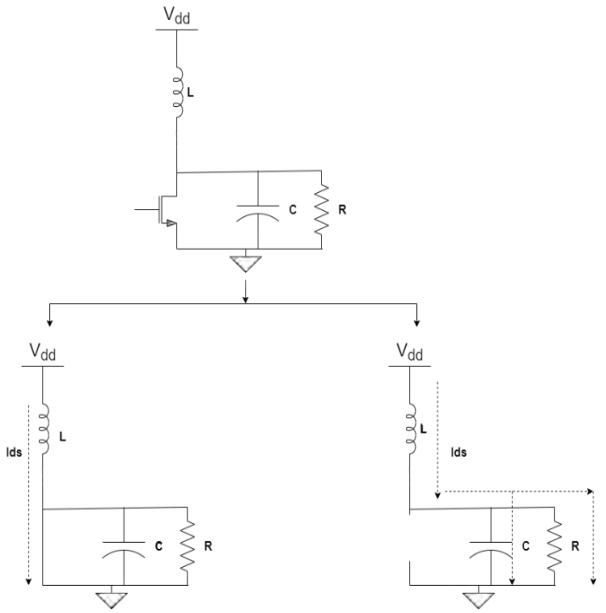


Fig. 5. Equivalent circuit of class E amplifier [2]

When the active switch turns on the current flows through choke inductance L, and when the switch is turned off the current flows through the shunt capacitance and load resistance denoted as C and R respectively in figure 5. The circuit works as RLC parallel resonant circuit when the switch is open with a resonant frequency given as

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{7}$$

The switching frequency has to be similar to the resonant frequency to ensure proper charge and discharge of energy between the inductor and capacitor. A duty cycle of 50% is also required to ensure no overlap between drain voltage and current. The ideal waveform of drain voltage and current is shown in figure 6.

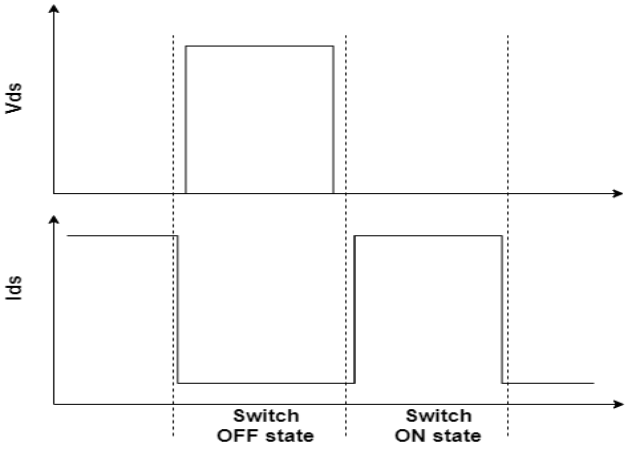


Fig. 6. Drain voltage and current waveform across an ideal switch of Class E SMPA[1]

Moreover, a series resonant circuit with a resonant frequency equal to the input frequency is placed before the load resistance as in fig 1, to get a sinusoidal waveform at the output.

F. Negative Impedance Method

The negative impedance method for linearization of amplifiers was first described by R.Wu et al in [16]. Later on, M.T. Ali et al in [10] modeled his negative feedback amplifier with negative impedance linearization using the Volterra series. Again, in [12] R. Wu describes the linearization scheme using the close loop differential amplifier shown below in fig 6.

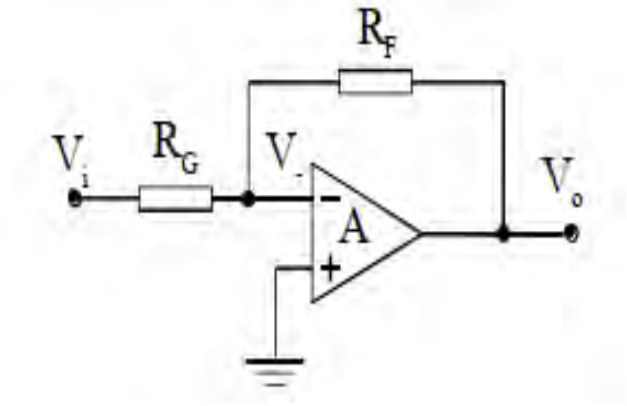


Fig. 7. Negative feedback differential amplifier [12]

The gain equation for figure 10 can be written as

$$-\frac{Vo}{RF} = \frac{Vin}{RG} \tag{8}$$

Equation 8 is only valid in ideal cases. Hence considering nonlinearities, equation 8 can be rewritten as according to [12],

$$-\frac{Vo}{RF} - \frac{Vo}{A}\left(\frac{1}{Zi} + \frac{1}{RF} + \frac{1}{RG}\right) = \frac{Vin}{RG} \tag{9}$$

From the left-hand side of equation (9), the second term is denoted as distortion current, id [12].

$$id = -\frac{Vo}{A}\left(\frac{1}{Zi} + \frac{1}{RF} + \frac{1}{RG}\right) \tag{10}$$

This distortion component, id can be addressed using the negative impedance method which generates anti-distortion current, iad. Figure 8 shows the implementation of this method which can be found in [12].

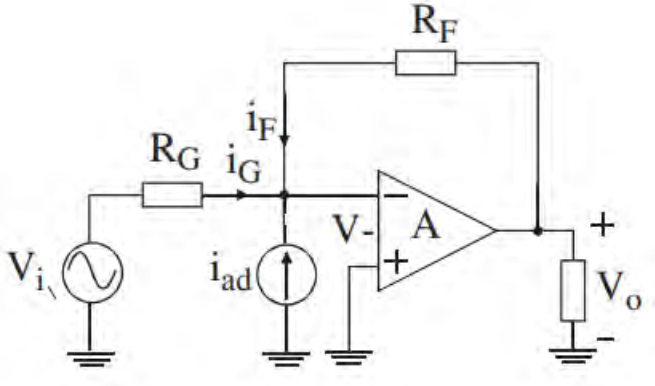


Fig. 8. Conceptual implementation of negative impedance method [12]

According to R.Wu in [12], if this anti-distortion current is made equal to the distortion current non-linearities should cancel out.

From fig 11, by applying KCL at the input node, the anti-distortion current stands as,

$$iad = ii - iG - iF \quad (11)$$

Hence, by measuring the current from the input source, iG, feedback current, iF, and the current through the inverting input terminal ii, the anti-distortion current can be found out.

IV. Simulation Results and Analysis

A. Performed Simulations

In this section, the results of the performed simulations are analyzed both before and after applying the linearization method. The performed simulations are DC analysis, Transient analysis, and Periodic Steady-state analysis. Later on, a mathematical model is also presented which was done with the help of MATLAB.

B. Assumptions

As in design, a number of considerations and assumptions were taken into account before going into the details of simulation results. The design considerations are stated below.

- Passive components that are used are considered to be ideal
- The design is tested for only a sinusoidal wave input with 1.4V swing and 1.24 V DC offset running at 2GHz
- The results that are presented are all pre-layout simulation
- The condition of the simulation was in typical process corner at 27ºC temperature with a nominal supply voltage of 2.5 V

C. Simulations on the Driver stage

At first DC simulation was performed to find out the amount of hysteresis was added to the design. The resultant hysteresis curve is shown in figure 9.

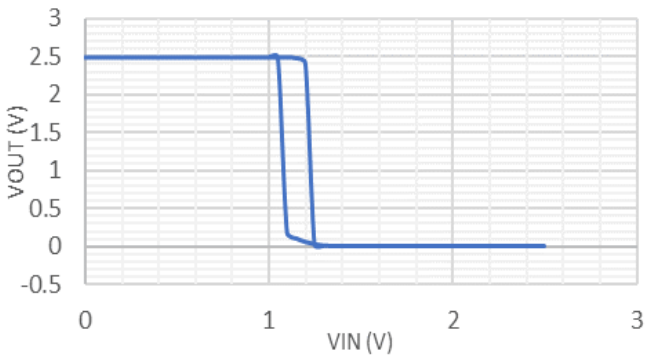


Fig.9. Hysteresis of Schmitt trigger

The curve in Figure 9 shows the output hysteresis when the input is swept from 0 to supply voltage, VDD. The RF signal that is coming from the input side is prone to noise. Having a hysteresis provides different tripping points which help to remove unwanted switching at the output of the driver and eliminating noise that would go into the power stage of the designed amplifier.

D. Testbench

A conceptual diagram of the class E amplifier testbench without linearization is presented in figure 10.

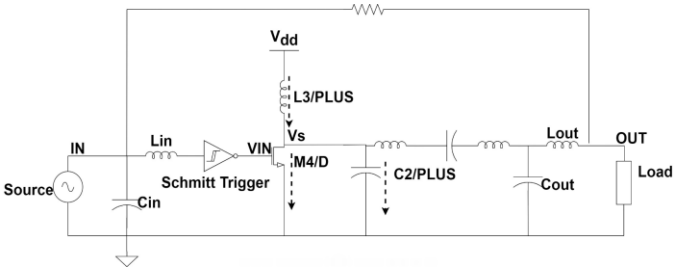


Fig. 10. Conceptual diagram of the simulated testbench

In figure 10, the source and load impedance were 50 ohms, and the feedback resistance was chosen to be 200k. The performed simulations on this testbench are transient analysis and PSS analysis.

E. Transient Analysis

In order to observe the output waveforms at various nodes transient analysis was performed. The resultant waveform is shown below in figure 11.

In figure 11, both external and internal waveforms of voltage and current are presented. The probing points are highlighted in figure 10. From the top, the solid VIN curve shows the square output of the Schmitt trigger driver for the input stated as IN shown in a dashed sinusoidal curve. Next, the curve denoted as L3/PLUS shows the waveform of current through the choke inductor which rises slowly to the peak when the NMOS turns on i.e., VIN is high. Again, M4/D and C2/PLUS waveforms are current waveforms of drain and shunt capacitor respectively. The flow of drain current is high whenever the VIN signal is high and when VIN is low the drain current is reduced and the current starts to flow through the shunt capacitor which is shown in the dashed waveform denoted as C2/PLUS. Moreover, the voltage across the switch or NMOS, denoted as Vs in the waveform, reaches its maximum value only when the VIN signal is low, otherwise, it stays at a minimal magnitude. Thus, by observing the waveform of drain current M4/D and drain voltage Vs, it is found that there is little overlap which is the basic functionality of class E amplifier. The overlap that is present will contribute to power dissipation.

F. Periodic Steady State Analysis

The periodic steady state or PSS analysis was performed on the class E amplifier to find output several measurements such as output power, output power gain, and most importantly linearity test from IIP3 curve. This simulation was done using harmonic balance engine with consideration of five harmonics at the output.

The output frequency domain plot of output power and gain is presented below in figure 12.

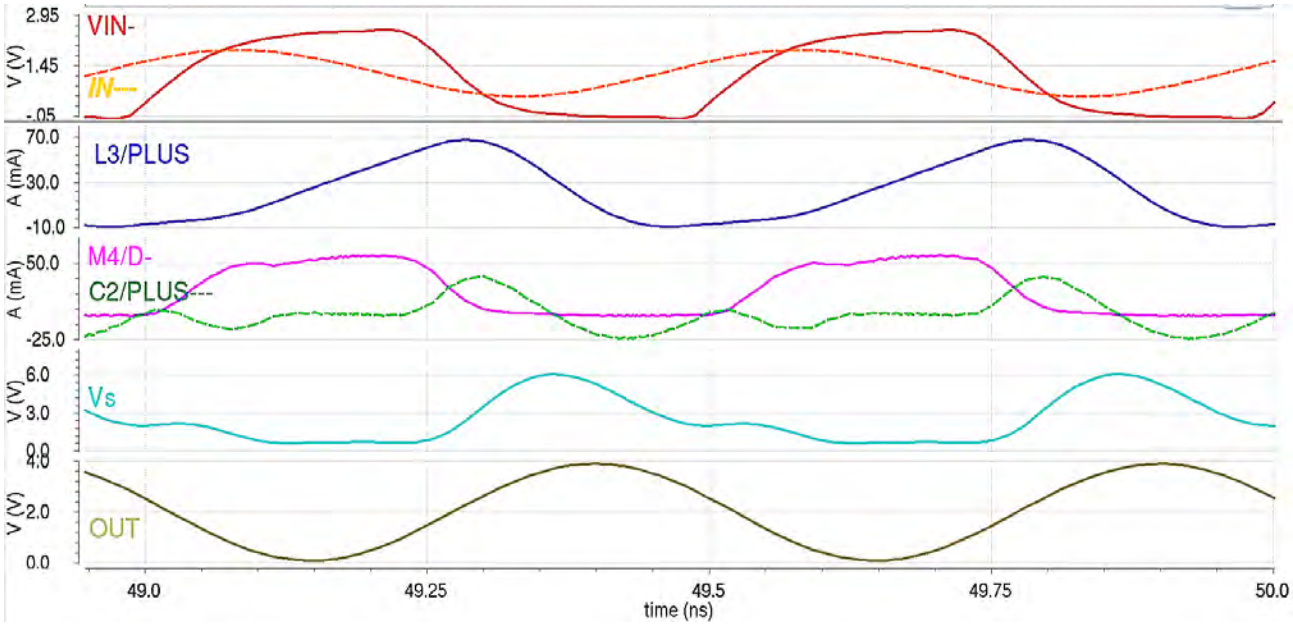


Fig. 11. Transient analysis waveforms of class E amplifier

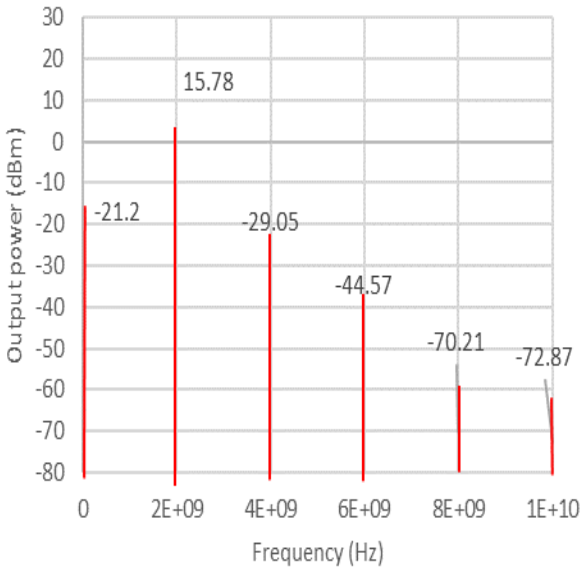


Fig. 12. Output power measurement

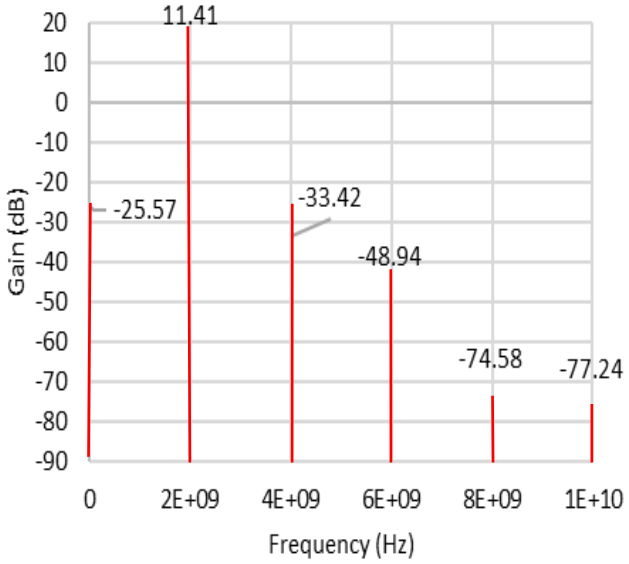


Fig 13. Output power gain in dB10

The measurement from figure 12 shows that the output power was found to 15.78dBm at the fundamental component.

The gain in power at the fundamental is shown below in figure 13. The gain was calculated to be 11.41dB with respect to an input power of 6dBm.

Moreover, during the PSS analysis power added efficiency was also measured and the simulated results are presented below in figure 14.

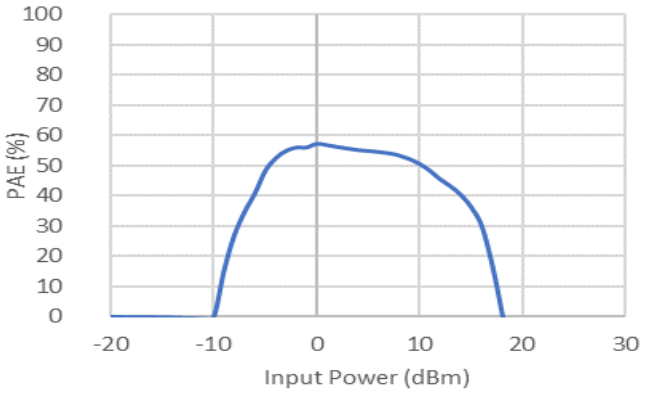


Fig. 14. Power added efficiency plot with respect to input power

The PAE plot shown in figure 14 was measured by sweeping the input power from -20dBm to 30dBm. The maximum efficiency was found to be around 57%. The main source of power reduction is the overlap drain voltage and current which is observed in transient waveforms shown in figure 11.

G. Linearity test before applying linearization

As a measure of linearity Input referred Intercept Point of 3rd order frequency (IIP3) curve was chosen as it shows a plot of output power against the input power of both 1st and 3rd order frequencies and their intercepting point of linear approximation curve. The following figure shows the IIP3 curve before applying linearization.

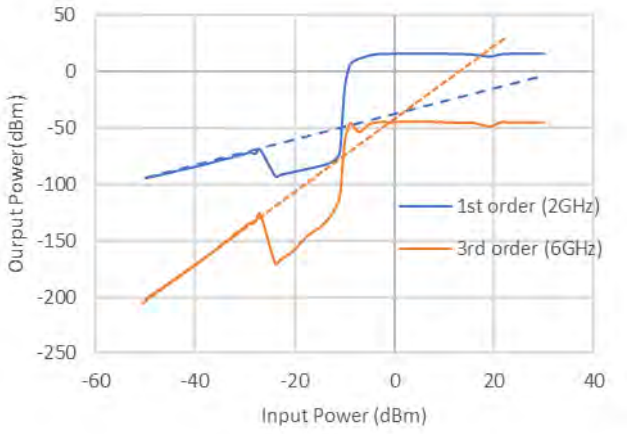


Fig. 15. IIP3 curve before application of linearization

From figure 15 it is seen that; the curve shows nonlinear behavior which is expected for a switch-mode power amplifier. The dashed line is the linear approximation of the curves and they intercept at the input power of 3.7dBm. Hence, the input referred intercept point is 3.7dBm. Moreover, it is also observed that the amplifier does not have any usable gain below -10dBm of input power.

H. Implementation of negative impedance

The negative impedance linearization was implemented on the following testbench shown in figure 16.

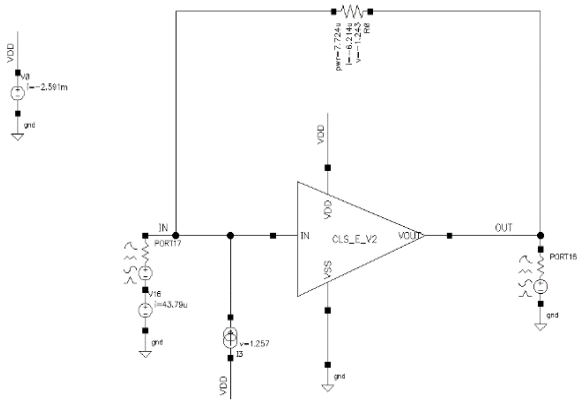


Fig. 16. Test bench of negative impedance linearization

In figure 15, the instance named “CLS_E_V2” is the class E amplifier which has a feedback resistance of 200K. At the input node, a current source is present which supplies the anti-distortion current. The magnitude of this current was estimated according to equation (11). Later on, it was further tuned to get better results. The final value of the current was found to be 40uA. After applying the anti-distortion current, the same simulations as shown previously were performed. Apart from linearity improvement, all the results seem to be the same. The following figure shows the IIP3 curve after applying the linearization scheme.

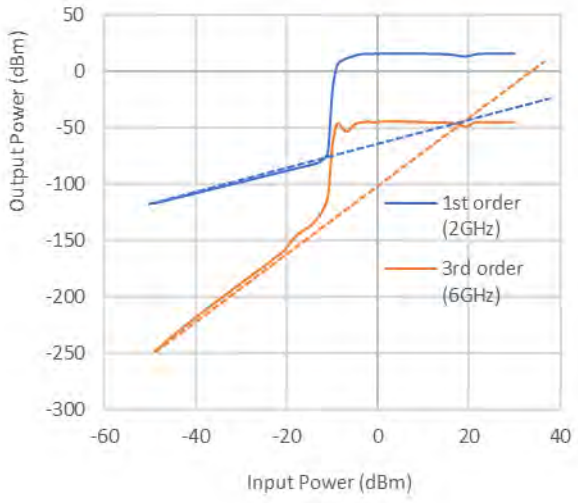


Fig. 17. IIP3 curve of 1st and 3rd order frequencies after applying linearization

It is observed that in figure 17 the intercepting point is at around 17.86dBm referred to input which was previously at 3.7dBm. Hence there is an improvement of around 12.08dBm.

I. Final Specification

After running the simulations both before and after applying the linearization scheme, it is found that the linearity has improved by 12.08dBm as seen from the IIP3 curves from figure 15 and figure 17. The final achieved specification of the designed amplifier along with linearization is shown in table III.

TABLE III. specification table

Specification (unit)	Value
Supply voltage (V)	2.5
Fundamental Frequency (GHz)	2
Output power at fundamental (dBm)	15.78
Power gain at fundamental (dB)	11.41
PAE (%)	54-57
IIP3 before linearization (dBm)	3.7
IIP3 after linearization (dBm)	17.86

J. Performance Comparison

The relevant performance parameters of the designed amplifier were compared against some previous works that are shown in Table VI.

TABLE IV: specification and comparison with previous studies

Ref	Transistor model	Frequency (GHz)	Gain (dB)	PAE (%)
[20]	GaN HEMT	1.9GHz	10	57-62
[21]	GaN HEMT	2-2.5GHz	10-13	71-74
[22]	GaN HEMT	0.9-2.2GHz	10-13	63-89
[23]	GaN HEMT	0.9-2.3GHz	7.5-13	57-88
This work	BSIM3v3	2 GHz	11.4	54-57

The comparative analysis shows that BSIM3v3 model shows similar performance as GaN HEMT technology in terms of gain and PAE. The only drawback is that BSIM3v3 is low-power MOSFET. Even so, it may perform well enough for lower power applications.

K. Mathematical Model

The mathematical model was designed from the data found from the IIP3 curves. The IIP3 curves shown in figure 15 and figure 17 are actually the transfer characteristics of the designed amplifier both before and after applying linearization. Hence, a polynomial equation can be found by curve fitting analysis yielding the desired mathematical model. The curve fitting analysis was done with the help of MATLAB with data found from Cadence Virtuoso. The following figure 18 shows the fitted curve for both 1st and 3rd order frequencies after applying linearization.

From the fitted curves found in figure 18, a polynomial equation can be made. The following table shows the power coefficients up to 7th order of power for both 1st and 3rd order frequencies.

TABLE V power coefficient for 1st and 3rd order frequencies before linearization

Input power order	Coefficients for 1st order frequency (dBm)	Coefficients for 3rd order frequency (dBm)
Pin^0	14.6591	-45.9544
Pin	2.0927	2.5196
Pin^2	0.7468	0.8828
Pin^3	-0.6383	-0.7653
Pin^4	-0.0887	-0.0978
Pin^5	0.0576	0.0680
Pin^6	0.0039	0.0040
Pin^7	-0.0023	-0.0027

The same approach can be taken for the fitted curve after linearization shown in figure 19. The results are presented in the following table shown in Table V.

TABLE VI: power coefficient for 1st and 3rd order frequencies after linearization

Input power order	Coefficients for 1st order frequency (dBm)	Coefficients for 3rd order frequency (dBm)
Pin^0	14.6385	-45.8482
Pin	2.0064	2.4239
Pin^2	0.7700	0.7937
Pin^3	-0.6173	-0.7349
Pin^4	-0.0930	-0.0853
Pin^5	0.0562	0.0652
Pin^6	0.0042	0.0033

It is observed by careful speculation, that the power order of table IV before linearization is up to the order of 7. On the other hand, the order of power coefficient after linearization found in table V is up to the order of 6. Moreover, the power coefficients seem less in table V than in table IV. Hence, this provides good evidence that linearity has improved by applying the negative impedance method.

According to table V and VI, the equation for both 1st and 3rd order frequencies would be,

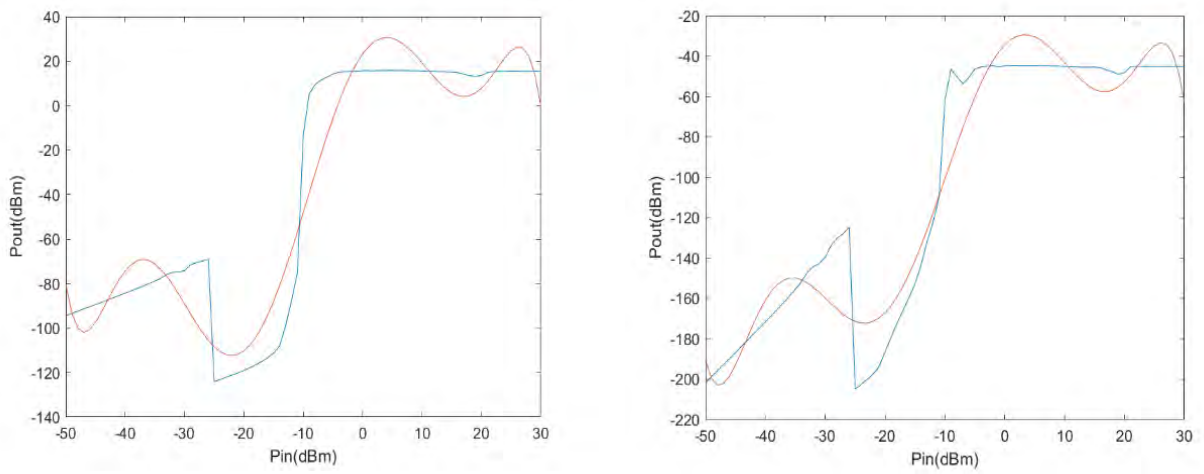
Before linearization,

For 1st order frequencies

$$Pout = 14.66 + 2.09Pin + 0.75Pin^2 - 0.64Pin^3 - 0.09Pin^4 + 0.06Pin^5 + 0.004Pin^6 - 0.0023Pin^7 \quad (12)$$

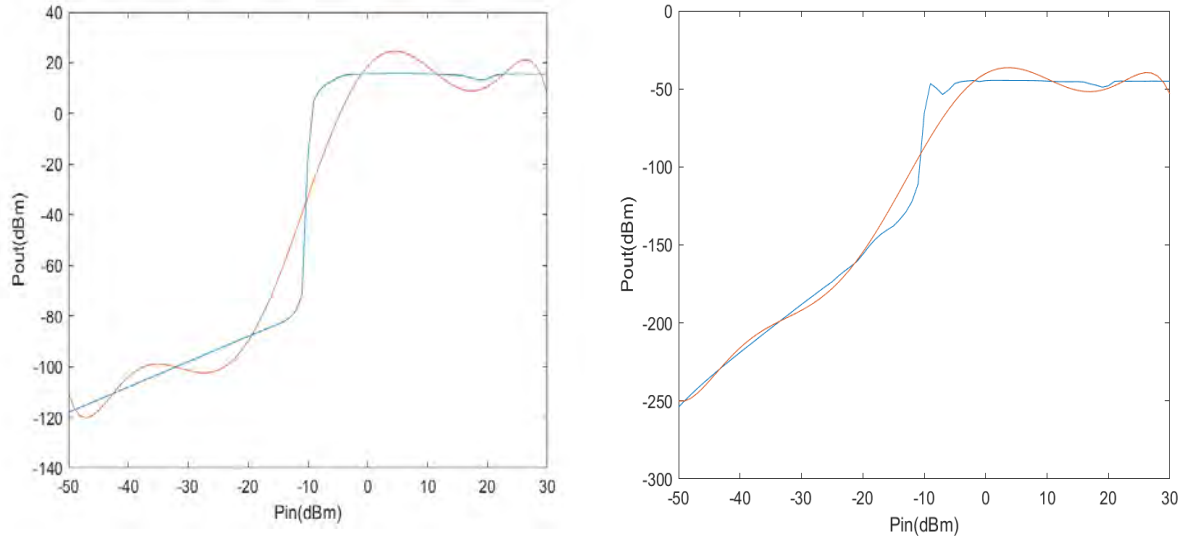
For 3rd order frequencies,

$$Pout = -45.95 + 2.52Pin + 0.88Pin^2 - 0.76Pin^3 - 0.1Pin^4 + 0.07Pin^5 + 0.004Pin^6 - 0.0027Pin^7 \quad (13)$$



(a) (b)

Fig. 18. original (blue) and fitted curve (orange) of (a) 1st order frequency (b) 3rd order frequency before linearization



(a) (b)

Fig. 19. original (blue) and fitted curve (orange) of (a) 1st order frequency (b) 3rd order frequency after linearization

After linearization,

For 1st order frequencies

$$Pout = 14.64 + 2.01Pin + 0.77Pin^2 - 0.62Pin^3 - 0.1Pin^4 + 0.05Pin^5 + 0.004Pin^6 \quad (14)$$

For 3rd order frequencies,

$$Pout = -45.84 + 2.42Pin + 0.8Pin^2 - 0.73Pin^3 - 0.08Pin^4 + 0.065Pin^5 + 0.003Pin^6 \quad (15)$$

V. FUTURE SCOPE

The goal of this work is to simulate and analyze the behavior of class E power amplifier with a linearization technique known as the negative impedance method. As this is a proof of concept, how the negative impedance is implemented in terms of circuit design is not presented in this work. There are several scopes for improvement in this work that can be done in the future. First and foremost, the device that is used is a 280nm CMOS process based on BSIM3v3 model. The design can provide much more power if more standard power MOSFET were used, typically LDMOS or more advanced processes like GaN HEMT. On the other hand, some design-related improvements can also be done. Firstly, the current source that is used is an ideal one. In real life, it can be implemented with a Wilson current mirror along with a bandgap reference circuit [18]. Another improvement can be done by a power management block known as multilevel

envelope tracking which can adjust the power supply according to necessity hence improving efficiency [19]. In order to get more robust and confident results, a physical custom layout of this work and post-layout simulation across different process corners, temperature, and supply can be done.

VI. Conclusion

The motivation of this work was to apply a simple design to linearize a highly nonlinear switch-mode power amplifier, class E amplifier. This work provides a proof of concept of linearizing a class E amplifier with a negative impedance method. As previously discussed, the class E amplifier is a switch-mode power amplifier where the active device is operated as a switch. On the other hand, the negative method was originally made for a differential amplifier which provides an anti-distortion current at the input of a feedback differential amplifier. According to the results that are shown in previous sections, the linearity parameter IIP3 should remarkable improvement keeping all other performance parameters such as output power, power gain, and PAE. This work also provides a mathematical model for the designed amplifier which also provides evidence on linearity improvement. Hence, it can be said that the negative impedance method can be a good candidate for the linearization of class E amplifiers.

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