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Design of a Robust ESD Protection Device using 6H-SiC Nano-Scale GGNMOS

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***Abstract*—With the continuous shrinking of the technological nodes and the introduction of new device concepts and materials, integrated circuits (IC) are becoming more vulnerable to electrostatic discharge (ESD) induced failures which is one of the major concerns in designing robust ICs. Therefore, to improve the reliability of the ICs against ESD-induced failures, extensive research efforts are being conducted. In this paper, we have presented a 6H-SiC based nano-scale grounded-gate NMOS (ggNMOS) ESD protection device and compared the results with the 3C-SiC-based ggNMOS. To design a robust ESD protection device, some critical device parameters, such as substrate doping concentration, source/drain doping concentration, drain to substrate contact spacing, and substrate contact resistance should be optimized. The ESD protection characteristics can be improved by utilizing the near punch-through effect. It was found that the trigger voltage and hold voltage are higher in 6H-SiC than the 3C-SiC having identical device parameters. 6H-SiC shows better voltage clamping performance as the turn-on resistance of 6H-SiC is smaller compared to the 3C-SiC material. Therefore, the results show that 6H-SiC has a better performance compared to 3C-SiC and due to its higher bandgap, and can be used as a good ESD protection device. All the simulations are carried out using the Silvaco ATLAS device simulator.**

Index Items*—*ggNMOS, snapback, parasitic BJT, ESD, TCAD, 6H-SiC, 3C-SiC, trigger voltage, hold voltage.

I. INTRODUCTION

Electrostatic Discharge (ESD) has become one of the major reliability issues in nano-scale integrated circuits. The damages caused by the ESD strikes can be catastrophic or minor. Catastrophic damage can destroy devices instantly. Minor damages are harder to detect instantly, but it causes gradual performance degradation and eventually leads to IC failures. Any time, from the beginning of IC fabrication to shipping, receiving, and the final phase of IC applications, whenever, an IC or any conducting materials are touched by a human, an ESD event may occur. To avoid ESD-induced damages, it is important to implement protection devices within the IC chips to shunt the ESD currents during an ESD strike. Therefore, on-chip ESD protection mechanisms are important to protect the internal circuitry of an IC against ESD strikes [1]. Based on the statistics of the ESD association in 2019, more than 25% of the electronic devices are destroyed by ESD strikes worth around 5 billion USD a year [2] [3].

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To protect electronic devices against ESD strikes and to improve the robustness of the ESD protection devices, many studies are being conducted all over the world. The operation of ESD protection devices is generally based on a technique known as snapback [4]. Several configurations such as gate-coupled NMOS (GCNMOS), grounded-gate NMOS (ggNMOS), silicon-controlled rectifier (SCR), substrate-triggered NNOS (STNMOS), and drain-extended NMOS (DeNMOS) are commonly used ESD protection devices [5-7]. The latch-up issue is the major limitation of SCR-based ESD protection devices due to its relatively large trigger voltage and small holding voltage [8] [9]. Further, substrate-triggered NMOS ESD protection devices are process technology-dependent [10]. Furthermore, gate-coupling NMOS forms a strong-inversion channel in the NMOS transistor due to coupled gate voltage. It makes the GCNMOS less effective to withstand ESD stresses [11]. Moreover, for the state-of-the-art CMOS technologies, an additional set of masks are required for both p and n-type of channel implantations and to achieve specific drift of a device making drain extended NMOS less lucrative [12].

Another ESD protection device based on ggNMOS is widely used in the industries due to CMOS technology compatibility, active discharge mechanism, low power dissipation, and simple construction [13].

SiC has multiple polytypes, out of which major polytypes are 3C-SiC, 4H-SiC, and 6H-SiC. These polytypes are widely used for commercial purposes. Therefore, researches are being conducted on these polytypes of SiC to cope with the ever-shrinking technological nodes and ESD failures. 3C-SiC is grown on Si wafers. But 3C-SiC is not as good as the single crystalline wafers which are currently available [14].

In this paper, we have presented a 6H-SiC based nano-scale grounded-gate NMOS (ggNMOS) ESD protection device with near punch-through source and drain junctions and compared the results with the 3C-SiC-based ggNMOS. 6H-SiC polytype has the potential to be used as an ESD protection device due to its high bandgap, high thermal conductivity, and high breakdown electric field. The effects of the variation of the significant device parameters, such as substrate doping concentration, source/drain doping concentration, drain to substrate contact spacing, and substrate contact resistance has been analyzed.

In section II, previous works based on SiC materials and some important terms of ESD protection devices have been discussed. Our proposed design structure has been explained, in section III. In section IV, simulation methodology has been discussed. The methodologies for the on-chip ESD protection circuit have been discussed in section V. In section VI, the ESD protection device using ggNMOS has been analyzed.

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We showed the results and discussions in section VII. In section VIII, we compared our results with the previously investigated result. Finally, in section IX, we concluded our studies of the ggNMOS ESD protection device.

II. LITERATURE REVIEW

ESD protection devices within an IC should satisfy the requirements of an ESD design window as shown in Fig. 1. The hold voltage (V_h) should be greater than the normal operating voltage (V_{DD}) with some safety margin, typically 25% of normal operating voltage, V_{DD}, to avoid the latch-up problem [15]. The trigger voltage (V_{t1}) should be less than the gate oxide breakdown voltage (V_{BD}) to ensure the reliability of the device. Under the normal operating condition, the ESD protection device should be in the off-state to ensure the normal operation of the IC. The ESD protection device faces permanent damage when the ESD voltage and current reach to second breakdown, also known as thermal breakdown [16]. Turn-on resistance (R_{on}) is the change in drain voltage to the change in drain current ($\Delta V/\Delta I$) when the ESD protection device is turned-on during an ESD event. Smaller turn-on resistance not only indicates better voltage clamping performance but also reduce the Joule heat of an ESD protection device to improve current-handling ability. [17] [18].

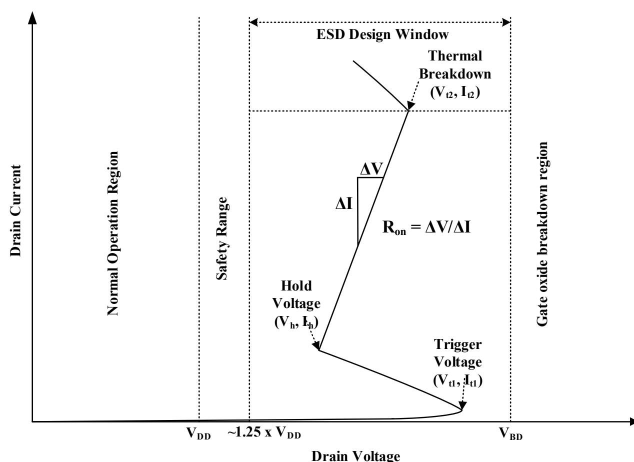

Fig. 1. ESD Design Window

ESD protection devices are primarily based on silicon material. However, silicon-based devices inherently have some limitations. Silicon-based devices have a maximum operating temperature typically below 150°C [19]. The bandgap of silicon at room temperature is 1.11 eV [20]. As silicon is a low bandgap material, the critical electric field required to start impact ionization is lower than silicon carbide material. Studies show that the breakdown voltage of silicon-based devices is around ten times smaller than silicon carbide-based devices [14]. Silicon carbide is a wide bandgap material that can function at an extremely high temperature up to 600°C [21]. Being a wide bandgap material, silicon carbide also has a low turn-on resistance, and fast switching speed [22].

Therefore, due to the continuous scaling of the semiconductor devices and the inherent limitation of silicon material, a significant number of researches are being conducted to use high bandgap materials, such as silicon carbide, beyond the limits of silicon. Silicon carbide is a promising wide bandgap material that attracts many researchers to design ESD protection devices with improved robustness. ESD protection circuit using 4H silicon carbide material that has good high-temperature and low on-resistance properties based on ggNMOS for 70V applications is proposed [23]. A recent study shows that SCR structure based on 4H-SiC material can mitigate the strong-snapback phenomenon that usually occurs in SCR and showed low trigger, high holding voltage characteristics [21]. The physical properties and failure mechanisms of SiC MESFET during ESD stress are examined by using the human body model and transmission line pulse tests [18]. Failure study of SiC junction barrier Schottky diodes under the human body model was also investigated [24]. The ESD characteristics of lateral-diffused MOS, silicon-controlled rectifier, and NMOS were investigated to develop the ESD protection structures based on SiC [25]. The robustness of silicon carbide MOSFET under the ESD strike has been studied based on photon emission and spectral photoemission technique [26] [27]. The safe operating area of the low voltage SiC-based NMOS transistor was reported [28]. The dependence of temperature on the diode, ggNMOS, and diode-string ESD protection structures which are fabricated in a 28nm CMOS technology was examined [29].

III. PROPOSED DEVICE STRUCTURE

Fig. 2 shows the proposed structure used for both the 6H-SiC and 3C-SiC-based ggNMOS ESD protection devices. The gate length of the devices is 28nm. The material, 6H-SiC, and 3C-SiC are used as the substrate of the devices. The substrate of both the devices is p-doped, and the sources and drains are heavily n-doped. Substrate contact is connected to a heavily doped p-type layer to produce ohmic metal-semiconductor contact as shown in Fig. 2. The length of the drain, source, and substrate are taken sufficiently large so that the device can withstand a significant amount of current. Shallow trench isolation (STI) is used to avoid leakage current among the adjacent devices. It also helps to prevent doping to increase locally. Thus, the current gain of the lateral parasitic NPN BJT does not degrade [30]. To reduce the high trigger and hold voltages of the SiC device due to its wide bandgap, near punch-through effect is utilized. It helps to control the trigger and hold voltages of the ggNMOS devices by changing the key device parameters, such as substrate doping concentration, source/drain doping concentration, drain to substrate contact spacing, and substrate contact resistance.

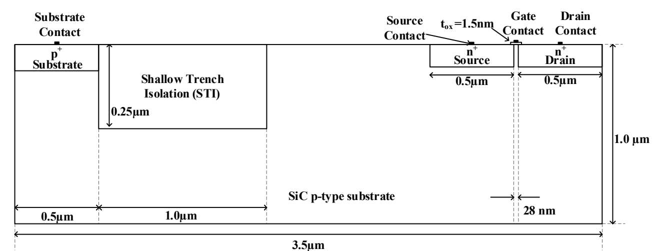

Fig. 2. A cross-sectional view of the proposed SiC-based ggNMOS device

Table I shows the fixed device parameters used in the SiC-based ggNMOS structure.

TABLE I. FIXED DEVICE PARAMETERS USED IN THE GGNMOS STRUCTURE

Device Parameters	Values
Channel length, Lg	28 nm
Gate oxide thickness, t_{ox}	1.5 nm
Drain, source, substrate length	0.5 µm
STI length	1.0 µm
Total device length	3.5 µm
Device height	1.0 µm

Fig. 3 shows the ESD protection circuit using ggNMOS. The ggNMOS ESD protection devices are placed on each I/O pad. During an ESD event, high drain voltage causes high drain current to flow through the ggNMOS. Therefore, by providing a safe path for the ESD current to flow to the ground, ggNMOS can protect the IC chip.

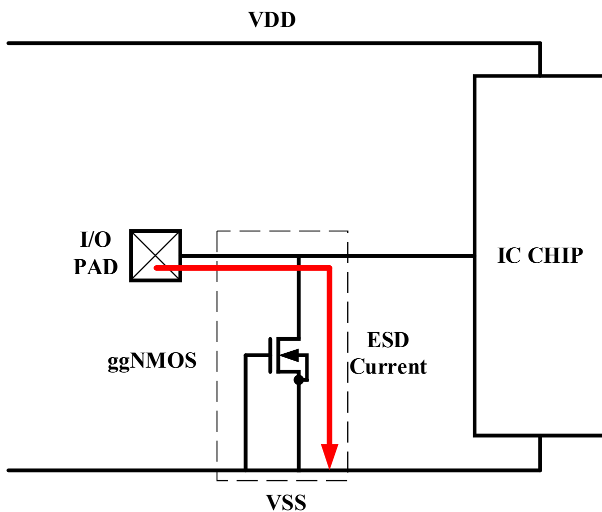

Fig. 3. The ESD protection circuit using ggNMOS

IV. SIMULATION METHODOLOGY

Silvaco ATLAS is a commercial technology computer-aided design (TCAD) device simulator tool that is typically used to simulate the electrical characteristics of semiconductor devices. In this paper, it is used to investigate the device performance of SiC-based ggNMOS under an ESD strike. To simulate a device correctly, five groups of statements must be defined in exact order. They are structure specification (mesh, region, electrode, doping), material models specification (material, models, contact, interface), numerical method selection (method), solution specification (log, solve, load, save), and result analysis (extract, tonyplot) [31].

A. *Mesh Strategy*

As the ggNMOS ESD protection devices are based on snapback behavior, it is important to define the mesh correctly in order to converge the numerical solution and to get improved precision on the results. Denser meshes are used in the contact region, the edges of the source, drain, substrate, and STI regions to improve the divergence problems of the simulation. Fig. 4 shows the mesh structure for 6H-SiC. The mesh structure of 3C-SiC is the same as 6H-SiC.

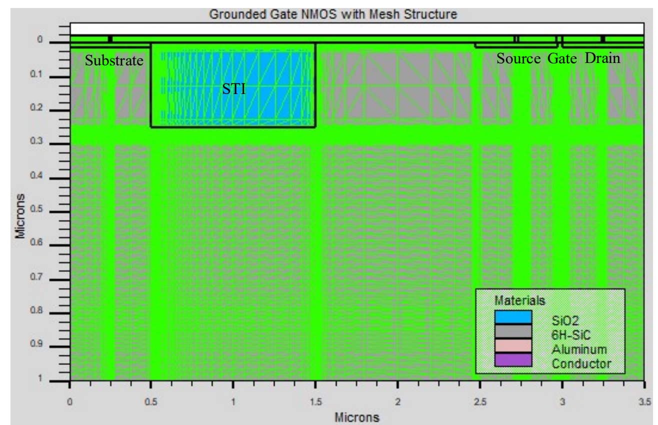

Fig. 4. The mesh structure of 6H-SiC ggNMOS

B. *Physical Models*

To model ESD stress properly, models related to carrier mobility, carrier statistics, impact ionization, and recombination should be introduced.

The following physical models are used in the simulation:

1. Fermi: To model carrier statistics Fermi-Dirac model is used.
2. BGN: As the S/D regions are heavily doped, the bandgap narrowing model is incorporated.
3. CONSRH: Carrier generation and trap-assisted recombination are modeled using Concentration-Dependent Shockley-Read-Hall [32]. The carrier lifetime is fixed.
4. CVT: Lombardi CVT model includes the effects of temperature, the dependence of mobility on doping concentration, carrier to carrier interaction, and both the perpendicular and transverse electric field [31] [33].

Gummel and Newton methods are used. The simulation will first run using Gummel iterations and then move to Newton iteration if Gummel iteration cannot successfully converge. To model the impact ionization, Selberherr's model is used. An algorithm based on automatic curve tracing that uses a dynamic load line is used [34].

V. METHODOLOGIES FOR ON-CHIP ESD PROTECTION

To improve the robustness of the ICs, on-chip protection for ESD should be implemented that possesses the following characteristics [35]:

a. The ESD protection circuit should offer a low-impedance path from pads to the ground to give off the static charge gathered when an ESD event occurs.

b. The voltage of the pads should be clamped at a level that is lower than the dielectric breakdown voltage of the transistors during an ESD event.

c. The ESD protection circuit should be such that it causes a minimum effect on the operation of the circuit to be protected by providing a high impedance and a low capacitance during the normal operation.

A pad-based ESD protected input/output circuit is shown in Fig. 5.

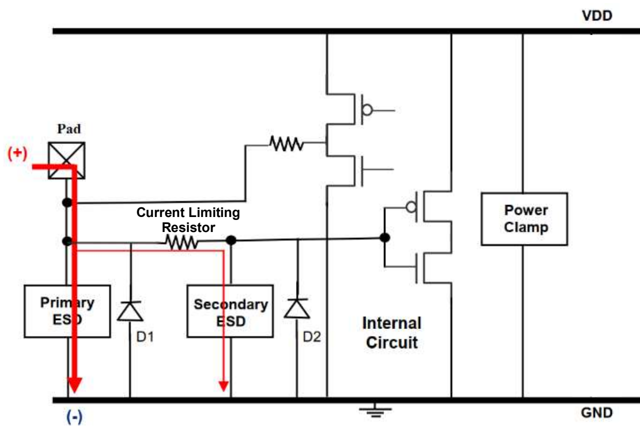

Fig. 5. A pad-based ESD protected input/output circuit [35]

Usually, an ESD protection circuit is comprised of a primary ESD protection stage, a current-limiting resistor, and a secondary ESD protection stage. ESD protection circuits should be placed in the vicinity of the pads as they are most vulnerable to the ESD stress if the protected circuits are placed far apart. The primary ESD protection stage is used to clamp the pad voltage and bypass the ESD induced current. The secondary ESD protection circuit is the downscaled version of the primary ESD protection stage [35]. By reducing the drain voltage of the secondary ESD protection transistors and by limiting and keeping nearly constant current, the resistor can withstand high voltage caused by ESD stress. To sense the ESD stress faster, the primary ESD protection circuit should be placed near the I/O pads [35]. In Fig. 5, ESD current shunt from the I/O pad to the ground is shown on the onset of the positive ESD event. In case of negative ESD stress from I/O pad to V_{DD}, diode D1 and D2 in addition to the power clamp provide the ESD current path.

VI. ESD PROTECTION DEVICE USING GGNMOS

ESD protection devices aim to clamp the voltage to a safe level for the internal circuitry and to shunt the high ESD current while being able to withstand the high energy ESD stress. The lateral parasitic BJT formed in the ggNMOS device dominates the ESD characteristics which have high current handling capability. Fig. 6. shows the lateral parasitic BJT formation in the ggNMOS transistor where the source, drain, and substrate of the device are emitter (E), collector (C), and base (B) of the parasitic BJT respectively. The substrate of the device has finite effective resistance, R_{sub}.

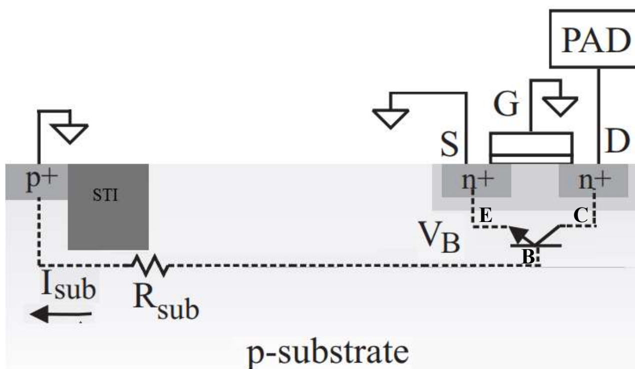

Fig. 6. Lateral parasitic BJT formation in the ggNMOS transistor

To ensure the NMOS is being off under the normal operating condition, the gate is grounded and hence the name grounded-gate NMOS (ggNMOS). The source-substrate/drain-substrate PN junctions are reversed biased. As both the PN junctions are reversed bias, in normal operating conditions, the lateral parasitic BJT is off. Therefore, there will be a negligible amount of substrate current, I_{sub}, and a slight voltage drop across the substrate-source junction. During an ESD event, the capacitance at the drain terminal of the ggNMOS charges up by ESD induced current. Consequently, a significantly high electric field forms across the substrate to drain junction. Due to this high electric field, impact ionization initiates leading to the start of the avalanche multiplication process. The substrate current, I_{sub} increases as the SiC lattices are hit by high energy carriers that can generate more electron-hole pairs. These newly developed electron-hole pairs become free carriers and again collide with SiC lattice to generate an increased number of electron-hole pairs. This creation of electron-hole pairs from the free charge carriers is known as impact ionization. As the substrate has effective resistance, the substrate current causes voltage drops at the substrate. As the drain current keeps on increasing during an ESD event, the substrate current also increases. At one point, the substrate voltage will be sufficiently large enough to turn on the lateral parasitic BJT and snapback occurs.

Substrate doping concentration which is one of the key parameters in designing robust ESD protection devices has a significant effect on snapback behavior. Higher doping concentration on the substrate means that the amount of dopant is higher in the same region of the substrate. As there are more dopants for higher doping concentration, the carriers will collide with the SiC lattice more often than lower doping concentration. Consequently, the mean free path of the carriers will get reduced, resulting in loss of energy by colliding with the SiC lattice. Due to the decreased amount of energy of the carriers, a smaller number of carriers will have a sufficient amount of energy to take part in impact ionization. Therefore, the number of free carriers for higher substrate doping concentration will be lower. A smaller number of free carriers for higher doping concentration causes the substrate current to get smaller. Hence the voltage drop between substrate-source junction also reduces for the same amount of drain voltage. Therefore, to achieve the required amount of forward bias voltage between substrate-source junction, it takes more drain voltage for higher doping concentration to turn on the parasitic lateral BJT. Higher substrate doping concentration also decreases the effective substrate resistance, R_{sub} for the hole to flow from drain to substrate [36]. Due to lower R_{sub} for higher doping concentration, when substrate current, I_{sub} flows from drain to substrate, the voltage drops across substrate-source junction also get smaller for the same drain current resulting in delayed turn-on of the parasitic BJT and hence the ggNMOS need higher drain voltages to trigger for higher doping concentration [36] [37]. Increasing the substrate doping concentration, therefore, results in increasing hold and trigger voltage.

If the drain current keeps on increasing, heat is accumulated in the reverse PN junction as the produced heat cannot be quickly dissipated. Due to the temperature rise, the device will burn out. This phenomenon is known as a thermal breakdown. If the thermal breakdown of ggNMOS ESD

protection device is higher than the avalanche breakdown, as shown in Fig. 7(a), avalanche breakdown takes place at first, and then thermal breakdown. Unless the device reaches the thermal breakdown, it will not burn.

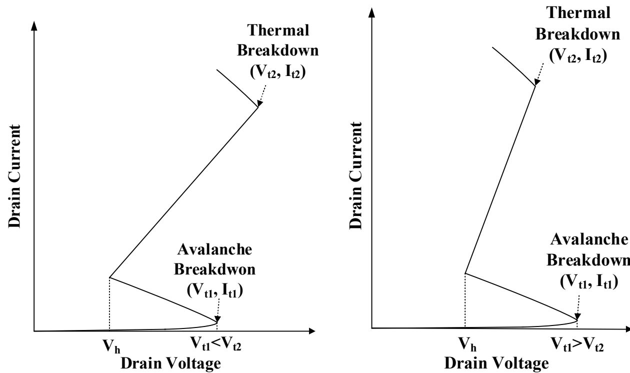

Fig. 7(a) Avalanche breakdown voltage is lower than the thermal breakdown voltage (b) Avalanche breakdown voltage is higher than the thermal breakdown voltage

On the other hand, if the avalanche breakdown voltage of ggNMOS is higher compared to the thermal breakdown, as shown in Fig. 7 (b), the device will be burnt before reaching the avalanche breakdown and should be avoided.

VII. RESULTS AND DISCUSSIONS

There are some major design parameters of grounded-gate nMOS that can be engineered to design reliable and robust ESD protection devices, such as substrate doping concentration, source-drain doping concentration, drain to substrate contact spacing, substrate resistance. The effects of these design parameters on the snapback behavior and the device performance have been analyzed.

A. *Effect of substrate doping concentration on 6H-SiC and 3C-SiC*

Three different substrate doping concentrations are used in this paper. The source/drain (S/D) doping concentration is taken as $2x10^{20}$ cm^{-3} for both the 3C-SiC and 6H-SiC. Table II shows the substrate doping concentrations used in this paper.

TABLE II. SUBSTRATE DOPING CONCENTRATIONS USED

Name	Doping Concentration (cm^{-3})
Substrate Doping Concentration I	$3x10^{18}$
Substrate Doping Concentration II	$4x10^{18}$
Substrate Doping Concentration III	$5x10^{18}$

The effects of the substrate doping concentration of 6H-SiC and 3C-SiC on ggNMOS snapback behaviors are shown in Fig. 8 and Fig. 12.

Fig. 8 shows that for the substrate doping concentration of $3x10^{18}$ cm^{-3}, the ggNMOS starts to conduct just before the snapback from around 7.1 to 7.75 drain voltage. This is because the reverse-biased drain-substrate diode initiates the avalanche breakdown. As avalanching diode has a declining impedance, any increase in drain voltage will also increase the base voltage of the parasitic BJT. Once the drain voltage increased by around 7.78 V, the base-emitter junction of the parasitic BJT becomes forward biased to turn on the parasitic BJT, and consequently, snapback occurs [36] [38].

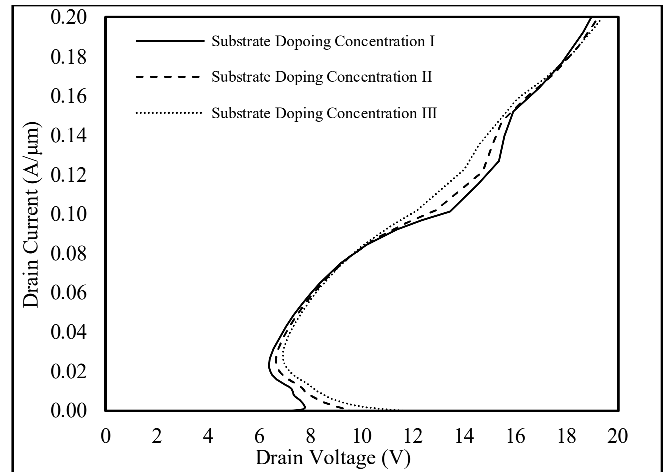

Fig. 8. Drain I-V curve for substrate doping concentration of 6H-SiC

As the substrate doping concentration is increased to $4x10^{18}$ cm^{-3}, the trigger and hold voltages are found to be 9.53 V and 6.64 V respectively. When the substrate doping concentration is further increased to $4x10^{18}$ cm^{-3}, the trigger and hold voltages also increase to become 11.65 V and 6.91 V respectively. Fig. 8 also shows that the turn-on resistance for all the substrate doping concentrations is almost similar till around 10 V. After that, for the substrate doping concentration of $5x10^{18}$ cm^{-3}, the turn-on resistance is the smallest among other substrate doping concentrations results in better voltage clamping performance and improved current-handling ability.

From the band diagram of the 6H-SiC ggNMOS as shown in Fig. 9, at the initial condition when there is no applied voltage, it can be seen that for higher doping concentration, the potential barrier for electrons between source to drain is higher. Due to this higher potential barrier, electrons require additional energy to lower the potential barrier between source to drain terminal to start the drain current flow. Due to the abrupt rise in drain current, the drain voltage decreases, i.e., snapbacks. Therefore, for higher substrate doping concentration, the ggNMOS will trigger later compare to the lower doping concentration.

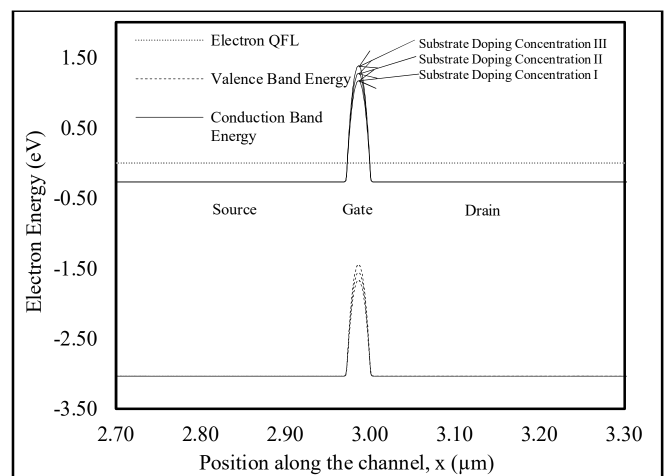

Fig. 9. Band diagram of the 6H-SiC ggNMOS at the initial condition

From Fig. 10, in the case of 6H-SiC having a substrate doping concentration of 4×10^{18} cm^{-3}, after snapback, the potential barrier between the source and drain terminal collapses and electron can easily from source to drain terminal. This leads to an increase in drain current and the drain voltage decreases. For the other two substrate doping concentrations, the potential barrier between the source and drain collapses in the same way, and electrons flow through the ggNMOS device.

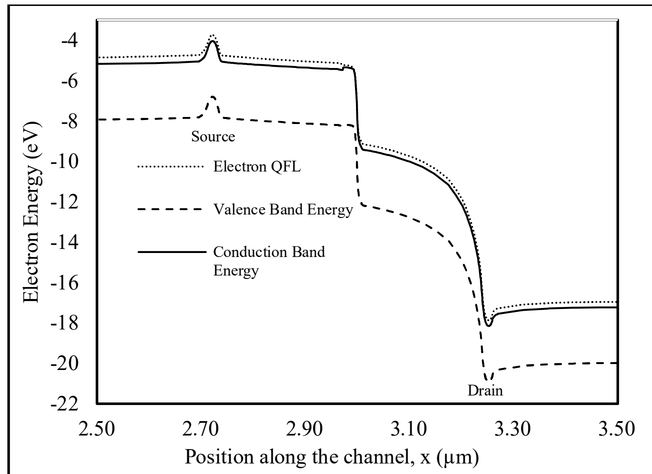

Fig. 10. Band diagram of the 6H-SiC ggNMOS after snapback

The electric field concentration of the 6H-SiC is shown in Fig. 11 (a) and Fig. 11 (b) for initial condition and after snapback respectively for the p-type substrate doping concentration of 4×10^{18} cm^{-3} and S/D doping concentration of 2×10^{20} cm^{-3}. From Fig. 11 (a) and Fig. 11 (b) it can be seen that after the snapback, there is an increased amount of electric field in the channel region than the initial stage. It is due to the fact that an increased amount of drain current flows through the channel region after the turn-on of the parasitic BJT formed in the NMOS structure.

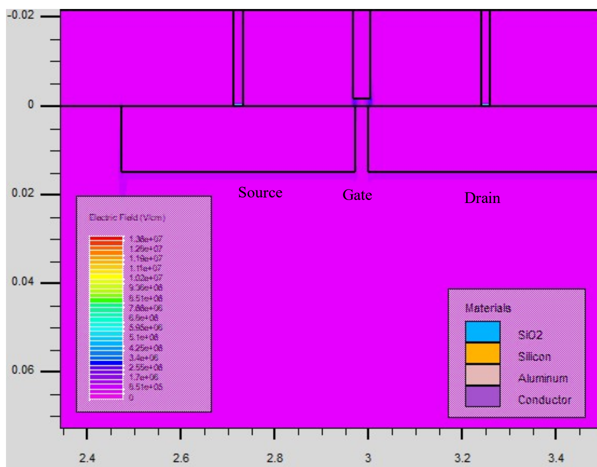

Fig. 11 (a). The contour of the electric field at the initial condition

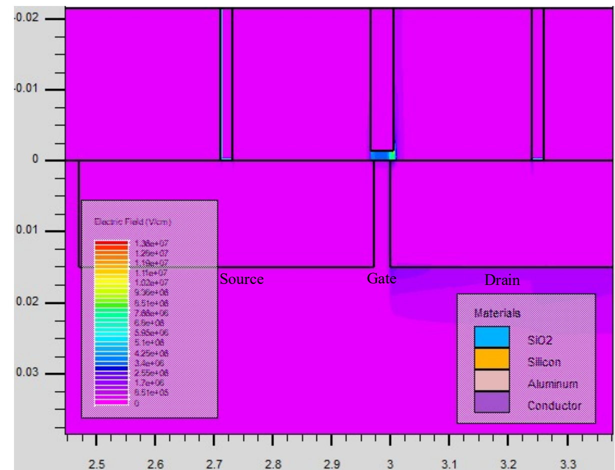

Fig. 11 (b). The contour of the electric field after the snapback

The snapback behavior for 3C-SiC is shown in Fig. 12. The physics behind the snapback is the same for both the SiC polytypes. The trigger voltages increase from 1.43V to 1.64V for the increase in substrate doping concentrations from 3×10^{18} cm^{-3} to 5×10^{18} cm^{-3}. The thermal breakdown voltages are 9.15 V, 9.99 V, and 10.73 V for the substrate doping concentrations of 3×10^{18} cm^{-3}, 4×10^{18} cm^{-3}, 5×10^{18} cm^{-3} respectively. The turn-on resistance of 3C-SiC for different substrate doping concentrations are similar. It means that their performance to clamp the voltage to a safe level will be almost the same.

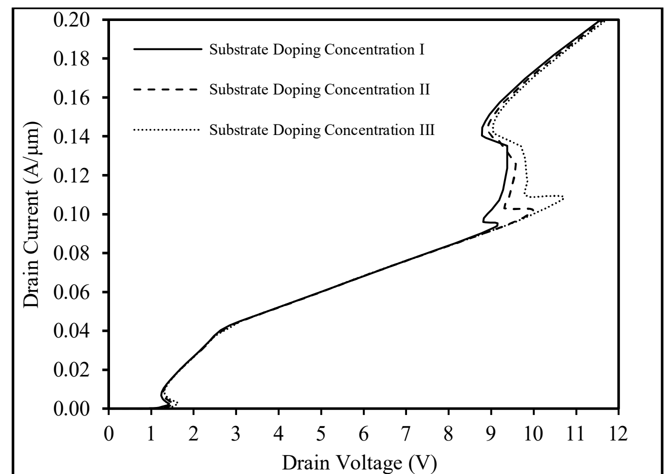

Fig. 12. Drain I-V curve for substrate doping concentration of 3C-SiC

Fig. 8 and Fig. 12 show that the trigger and hold voltage for 6H-SiC is much higher than the 3C-SiC having the same substrate doping concentration. This is due to the fact that the bandgap of 6H-SiC (around 3.0 eV) is much wider than the bandgap of 3C-SiC (around 2.4 eV) [14]. Hence, for 3C-SiC, the potential barrier between the source and the drain terminal is much smaller than its 6H counterpart as shown in Fig. 13.

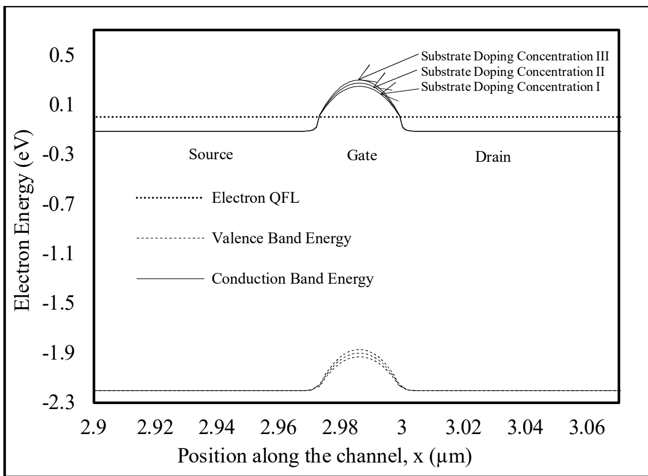

Fig. 13. Band diagram of the 3C-SiC ggNMOS at the initial condition

Due to this comparatively smaller bandgap of 3C-SiC, the trigger and hold voltage of 3C-SiC is much lower than the 6H-SiC. Table III shows the result summary of 6H-SiC and 3C-SiC in case of the variation of p-type substrate doping concentration while keeping the S/D doping concentration constant ($2x10^{20}$ cm^{-3}). The results are simulated up to the drain current of 200 mA/μm.

TABLE III. RESULT SUMMARY OF 6H-SIC AND 3C-SIC IN CASE OF THE VARIATION OF P-TYPE SUBSTRATE DOPING CONCENTRATION

Material	Substrate Doping Concentration (cm^{-3})	Trigger Voltage (V)	Hold Voltage (V)	Thermal Breakdown voltage (V)	Thermal breakdown current (mA/μm)
6H-SiC	$3x10^{18}$	7.78	6.38	No thermal breakdown is seen till 200 mA/μm	No thermal breakdown is seen till 200 mA/μm
	$4x10^{18}$	9.53	6.64	No thermal breakdown is seen till 200 mA/μm	No thermal breakdown is seen till 200 mA/μm
	$5x10^{18}$	11.65	6.91	No thermal breakdown is seen till 200 mA/μm	No thermal breakdown is seen till 200 mA/μm
3C-SiC	$3x10^{18}$	1.43	1.24	9.15	96
	$4x10^{18}$	1.54	1.28	9.99	102
	$5x10^{18}$	1.64	1.31	10.73	107

From Table III, it can be seen that for 6H-SiC, when the substrate doping concentration is $3x10^{18}$ cm^{-3}, the margin between the trigger and hold voltage is small and the turn-on resistance is also high. But in case substrate doping concentrations of $4x10^{18}$ cm^{-3} and $5x10^{18}$ cm^{-3}, the margins between the trigger and hold voltages are higher and the turn-on resistances are lower. Therefore, both $4x10^{18}$ cm^{-3} and $5x10^{18}$ cm^{-3} substrate doping concentrations can be a good choice for a 5 V ESD protection device with 25% safety margin. On the other hand, among other substrate doping concentrations of 3C-SiC, $5x10^{18}$ cm^{-3} shows the best device performance with moderate trigger and hold voltage margin and thermal breakdown voltage.

B. Effect of source-drain doping concentration on 6H-SiC and 3C-SiC

The effects of source/drain doping concentration on both the 6H-SiC and 3C-SiC are shown in Fig. 14 and Fig. 16. The substrate doping concentration is taken as $4x10^{18}$ cm^{-3}. By keeping the substrate doing concentration constant, the S/D doping concentrations are changed. The S/D concentrations are taken as $5x10^{19}$ cm^{-3}, $1x10^{20}$ cm^{-3}, $2x10^{20}$ cm^{-3}.

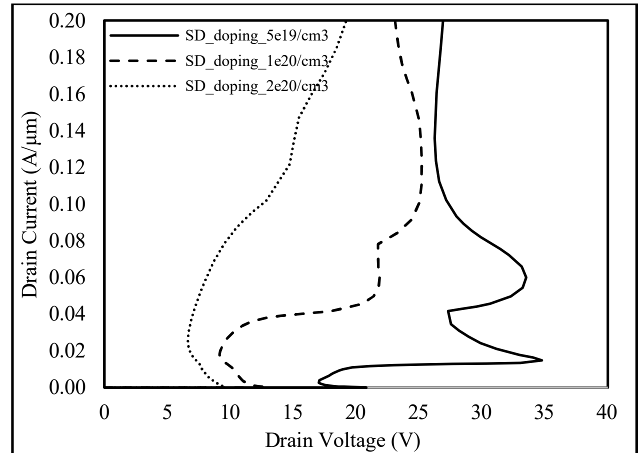

Fig. 14. Drain I-V curve for the variation of the source-drain doping concentration of 6H-SiC

Fig. 14. shows that for 6H-SiC, when S/D doping is $2x10^{20}$ cm^{-3}, the trigger voltage, V_{trig}, and hold voltage, V_{hold} are 9.53 V and 6.64 V respectively. The thermal breakdown does not occur even at 200 mA/μm drain current. By clamping the drain voltage to a sustainable voltage, the conduction of a significant current continues. This can save the device under protection and the ggNMOS itself can sustain more current without reaching to the thermal breakdown. The thermal breakdown is also considered as the boundary of the safe operating area [39]. Thus, S/D having a doping concentration of $2x10^{20}$ cm^{-3} is a good device if the normal operating voltage of the internal circuit is around 5V. If the S/D doping concentration is reduced to $1x10^{20}$ cm^{-3}, then the trigger and hold voltages become 12.94 V and the hold voltage occurs at 9.16 V respectively. The trigger voltage and hold voltage increase because when S/D doping is reduced for the same substrate doping concentration, the potential barrier increases from the Fermi level as shown in Fig. 15. Hence for reduced S/D doping concentration, electrons require additional energy to cross the p-type substrate potential barrier and start the conduction of the drain current.

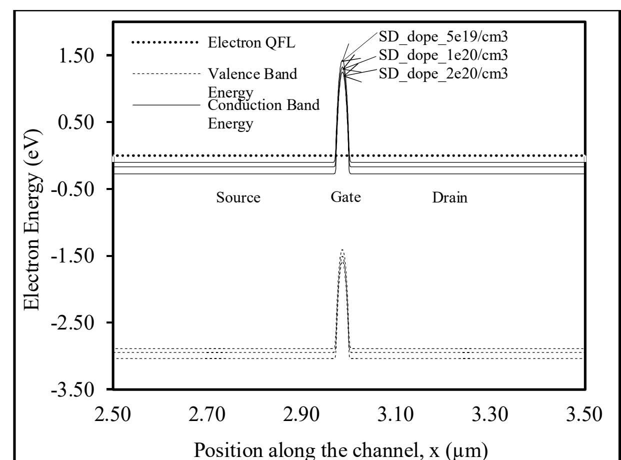

Fig. 15. Band diagram of the 6H-SiC for the variation of S/D doping concentration

In this case, thermal breakdown occurs at 21.85 V and 60 mA/μm drain voltage and current respectively. This device will permanently damage at 21.85 V drain voltage. If the S/D doping concentration is further reduced to 5x10^{19} cm^{-3}, the trigger and hold voltages increase further and the thermal breakdown takes place at 34.75 V and 15 mA/μm drain voltage and current respectively.

From Fig. 14, it can be investigated that for the same p-type substrate doping concentration, when S/D doping is 2x10^{20} cm^{-3}, the snapback occurs earlier but the device does not suffer thermal breakdown with a much higher drain current. On the other hand, when S/D doing is reduced, the device snaps back in much higher voltage, but the thermal breakdown happens at a smaller drain current. Smaller thermal breakdown current but higher thermal breakdown voltage indicates higher turn-on resistance ($\Delta V/\Delta I$). Large turn-on resistance is not good to clamp the voltage to a safe level. Therefore, here, in this case, S/D of 5x10^{19} cm^{-3} will not be a good ESD protection device.

Fig. 16. shows the snapback behavior of 3C-SiC under the same conditions as 6H-SiC. Increasing the S/D doping concentrations increase the trigger and hold voltages of the device. For S/D doping concentration 2x10^{20} cm^{-3}, the thermal breakdown occurs around 10 V and 102 mA/μm drain voltage and current respectively. But when the S/D doping concentrations are reduced the thermal breakdown current is reduced significantly. Thus, the turn-on resistances become high as the change in voltage with respect to change in current is high. Higher turn-on resistance indicates the declining performance of the device of its ability to clamp the voltage to a safe level in order to save the internal circuits [17].

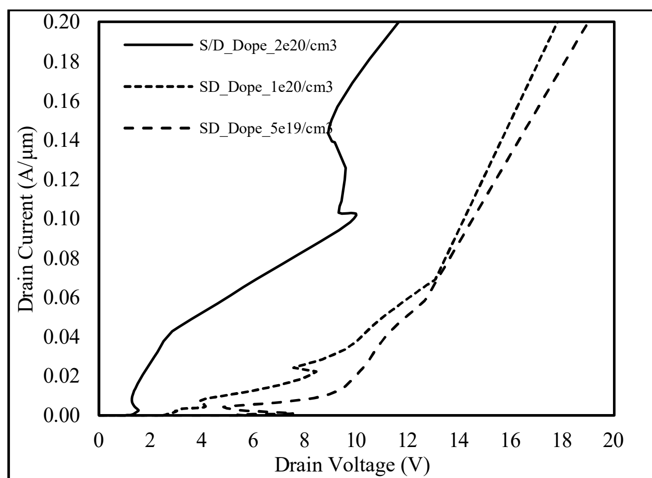

Fig. 16. Drain I-V curve for the variation of the source-drain doping concentration of 3C-SiC

Table IV shows the result summary of 6H-SiC and 3C-SiC in case of the variation of S/D doping concentration while keeping the p-type substrate doping concentration constant (4x10^{18} cm^{-3}). The results are simulated up to the drain current of 200 mA/μm.

TABLE IV. RESULT SUMMARY OF 6H-SIC AND 3C-SIC IN CASE OF THE VARIATION OF S/D DOPING CONCENTRATION

Material	S/D Doping Concentration (cm^{-3})	Trigger Voltage (V)	Hold Voltage (V)	Thermal Breakdown voltage (V)	Thermal breakdown current (mA/μm)
6H-SiC	2x10^{20}	9.53	6.64	No thermal breakdown is seen till 200 mA/μm	No thermal breakdown is seen till 200 mA/μm
	1x10^{20}	12.94	9.16	21.85	60.00
	5x10^{19}	20.8	17.05	34.75	15.00
3C-SiC	2x10^{20}	1.54	1.28	9.99	102.00
	1x10^{20}	4.15	3.94	8.44	22.00
	5x10^{19}	5.74	5.37	7.6	1.00

From Table IV, it can be seen that for 4x10^{18} cm^{-3} p-type substrate doping, 2x10^{20} cm^{-3} S/D doping concentration gives the best ESD protection having a good trigger and hold voltage margin and mild snapback. In addition to that, the turn-on resistance for 2x10^{20} cm^{-3} S/D doping concentration is also low indicating better voltage clamping performance [40]. On the other hand, the voltage margin between the trigger, and hold is very low for 3C-SiC. The thermal breakdown occurs at a lower voltage and current when S/D doping concentrations are decreased. The turn-on resistance of 3C-SiC is also higher than the 6H-SiC. Therefore, 3C-SiC is not as good as 6H-SiC as an ESD protection device.

C. Effect of substrate resistance on 6H-SiC and 3C-SiC

Effective substrate resistance, R_{sub} has a profound impact on the trigger and hold voltages of the snapback behavior. Substrate contact connection and its position directly impact the substrate resistance and consequently initiation of avalanche breakdown. Substrate resistance can be increased by either introducing lumped resistance between the ground and substrate contact or by moving away the substrate contact further from the drain contact [41].

a) Introduction of substrate contact resistance:

Fig. 17. and Fig. 18. show the drain I-V curve of 6H-SiC and 3C-SiC for the variation of external substrate contact resistance to the ground respectively. The variation is examined by introducing 200 Ω and 400 Ω substrate contact resistance to the ground. When substrate contact resistance is added, the effective substrate resistance increases which accelerates the avalanche breakdown. Thus, due to the increase in the effective substrate resistance, the base-emitter junction of the lateral parasitic BJT gets enough forward bias to turn it on for smaller drain voltages. Trigger and hold voltages are lower when the substrate resistance is 400 Ω than when there is no substrate resistance as shown in Fig. 17. and Fig. 18 [40]. The leakage current just before the trigger voltage is higher in 3C-SiC compared to the 6H-SiC.

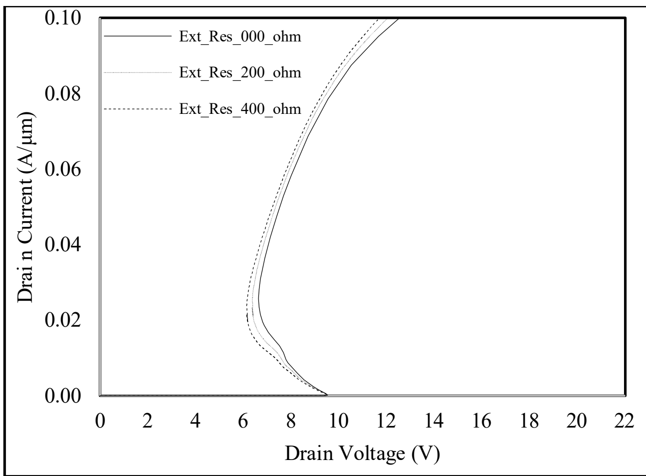

Fig. 17. Drain I-V curve of 6H-SiC for the variation of external substrate contact resistance to ground.

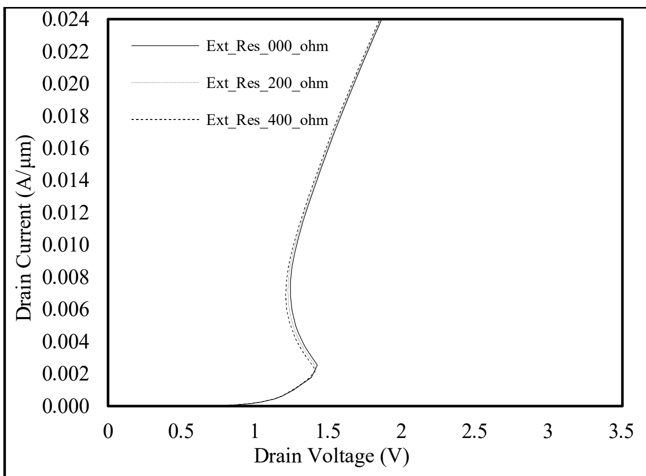

Fig. 18. Drain I-V curve of 3C-SiC for the variation of external substrate contact resistance to ground.

Table V shows the result summary of 6H-SiC and 3C-SiC when substrate contact resistance is introduced.

TABLE V. RESULT SUMMARY OF 6H-SIC AND 3C-SIC WHEN SUBSTRATE CONTACT RESISTANCE IS INTRODUCED

Material	Substrate Contact Resistance (Ω)	Trigger Voltage (V)	Hold Voltage (V)
6H-SiC	400	9.51	6.14
	200	9.52	6.37
	000	9.53	6.64
3C-SiC	400	1.40	1.20
	200	1.41	1.22
	000	1.43	1.24

From Table V, it can be showed that the increased substrate resistance can decrease the trigger and hold voltages of the device.

b) Moving substrate contact with respect to drain contact

If the distance between substrate contact and drain contact increases, then effective substrate resistance of the device increases as resistance is directly proportional to the length. The voltage drop across the base-emitter junction of the lateral parasitic BJT increases when the substrate resistance increases. Thus, the required amount of voltage drop across the base-emitter junction of parasitic BJT can be achieved with smaller drain voltage, consequently, the parasitic BJT turns on and the voltage of the drain terminal is reduced, i.e., snaps back. Fig. 19. and Fig. 20 show the drain I-V characteristics of 6H-SiC and 3C-SiC when the substrate contact position is changed with respect to the drain contact. It can be seen that when the distance between the substrate contact and drain contact increases, snapback occurs earlier.

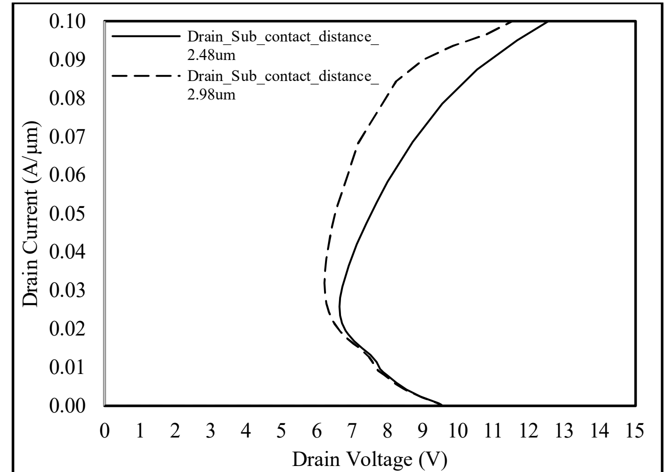

Fig. 19. Drain I-V curve of 6H-SiC for the variation of the distance of substrate contact with respect to drain contact

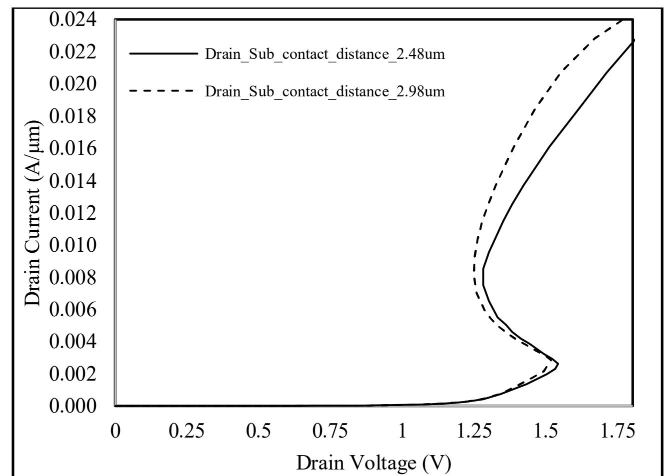

Fig. 20. Drain I-V curve of 3C-SiC for the variation of the distance of substrate contact with respect to drain contact

Table VI shows the result summary of 6H-SiC and 3C-SiC when substrate contact is moved with respect to drain contact.

TABLE VI. RESULT SUMMARY OF 6H-SIC AND 3C-SIC WHEN SUBSTRATE CONTACT IS MOVED WITH RESPECT TO DRAIN CONTACT

Material	Spacing between substate and drain contacts (µm)	Trigger Voltage (V)	Hold Voltage (V)
6H-SiC	2.98	9.51	6.21
	2.48	9.54	6.63
3C-SiC	2.98	1.51	1.24
	2.48	1.55	1.29

Table VI shows that the spacing between substrate and drain contacts affects the trigger and hold voltages of the device. An increased amount of substrate and drain contact

spacing results in higher substrate resistance, consequently have a lower trigger and hold voltages.

VIII. Comparison analysis

Table VII shows a comparative analysis between 28nm ggNMOS ESD protection device based on silicon at room temperature and the simulated SiC data. The substrate and S/D doping concentrations are considered to be $4x10^{18}$ cm^{-3} and $2x10^{20}$ cm^{-3} for silicon carbide.

TABLE VII. Comparison between the 28nm silicon-based ggNMOS [29] and 6H-SiC and 3C-SiC based ggNMOS (proposed design)

Parameter	[29]	Proposed design
Gate length	28 nm	28 nm
Trigger voltage	5.40 V	9.53 V (6H-SiC)
		1.54 V (3C-SiC)
Hold voltage	4.10 V	6.64 V (6H-SiC)
		1.28 V (3C-SiC)

Table VIII shows a comparative analysis between 4H-SiC and the investigated 3C-SiC and 6H-SiC.

TABLE VIII. Comparison between the 4H-SiC based ggNMOS [23] and 6H-SiC and 3C-SiC based ggNMOS (proposed design)

Parameter	[23]	Proposed design
Gate length	18 μm	28 nm
Trigger voltage	121.8 V	9.53 V (6H-SiC)
		1.54V (3C-SiC)
Hold voltage	81.6 V	6.64 V (6H-SiC)
		1.28 V (3C-SiC)
Normal operating voltage	70 V	Around 5 V (6H-SiC)
		Around 1.0 V (3C-SiC)

The minimum hold voltage of the ggNMOS should be 1.25 times the normal operating voltage of the internal circuitry [15]. Therefore, the normal operating voltage of the internal circuitry can be chosen around 5 V and 1 V for 6H-SiC and 3C-SiC respectively as the hold voltages are 6.64 V and 1.28 V of 6H-SiC and 3C-SiC. The reason behind the smaller trigger and hold voltages of our design is because the source and drain junctions of the ggNMOS are near punch-through. When the drain to substrate depletion region almost merges with the source to substrate depletion region, then the application of a small amount of reverse bias between the PN junction of drain and substrate can lead to current flow from drain to source. It is because the depletion regions will merge together. This effect is known as near punch-through. Therefore, the potential barrier between S/D gets smaller results in a smaller trigger and hold voltage compared to non-punch through devices.

IX. Conclusion

In this paper, a 6H-SiC based nano-scale grounded-gate NMOS (ggNMOS) ESD protection device with near punch-through source and drain junctions has been designed and compared the results with the 3C-SiC-based ggNMOS. The effects of the variation of design parameters such as substrate doping concentration, source-drain doping concentration, substrate contact resistance, and drain to substrate contact spacing of the ggNMOS ESD protection device have been investigated in this paper. It is found that an increased amount of p-type substrate doping concentration can lead to higher trigger and hold voltages of the silicon carbide devices. Increasing the S/D doping concentrations, decreases the trigger and hold voltages as the potential barrier between source to drain reduces. An increased amount of substrate contact resistance decreases the trigger and hold voltages as the effective substrate resistance increases. The spacing between substrate contact to drain contact of the device also affects the trigger and hold voltages of the device. By increasing the spacing between the substrate to drain contacts, the effective substrate resistance can be increased as resistance is directly proportional to the length. An increased amount of effective substrate resistance causes the parasitic BJT to turn on for lower drain voltages. The turn-on resistance is lower in 6H-SiC compared to the 3C-SiC. Thus, 6H-SiC has superior voltage clamping performance and improved current-handling ability by reducing the Joule heat of an ESD protection device than 3C-SiC during ESD strikes. In this paper, the result showed that both the 6H-SiC and 3C-SiC can be tailored to the desired voltages, ranging from low to high, to protect the internal circuitry while preserving the benefits of faster switching, low turn-on resistance, high electric field, and excellent high-temperature. Compared to 3C-SiC, 6H-SiC shows better performance in terms of ESD robustness and voltage clamping ability. These properties of 6H-SiC material make it a good ESD protection device.

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