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# Design and Evaluation of a 32-bit Carry Select Adder using 4-bit Hybrid CLA Adder

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***Abstract*—Adder circuits play a remarkable role in modern microprocessor. Adders are widely used in critical paths of arithmetic operation such as multiplication and subtraction. A Carry Select Adder (CSA) design methodology using a modified 4-bit Carry Look-Ahead (CLA) Adder has been proposed in this research. The proposed 4-bit CLA used hybrid logic style based logic circuits for Carry Generate ($G_i$) and Carry Propagate ($P_i$) functions in order to improve performance and reduce the number of transistors required. The modified 4-bit CLA is introduced as the basic unit for implementation of 32-bit CSA. The proposed design of hybrid CLA based 32-bit CSA has been compared with conventional static CMOS based 32-bit CSA and 32-bit Ripple Cary Adder (RCA) by conducting simulation using Cadence Virtuoso tools. Power consumption and delay in the proposed 32-bit CSA are found as 322.6 µW and 0.556 ns whereas those parameters in the conventional 32-bit CSA were 455.4 µW and 0.667 ns respectively. We have done all the simulation using Cadence Virtuoso 90 nm technology library.**

***Index Terms*—carry save adder, carry look-ahead adder, ripple carry adder, hybrid logic.**

## I. INTRODUCTION

THE rapid advancement and progress in electronics device has resulted in implementation of several highly intelligent and smart systems which have become essential in making our everyday life easy and comfortable [1-4]. These smart and intelligent systems require high-performance and cost-effective processors for which advanced circuit designs are of outmost necessity [5-7]. Therefore, Performance improvement of VLSI circuit designs plays a crucial role in modern circuits and systems [8].

One of the important subcomponent of VLSI system is digital adders. Designing of Adder has always gained high priority among researchers due to its extensive utilization in Arithmetic Logic Unit (ALU) in modern days [9]. Adders required in subtraction [10], multiplication [11], binary magnitude comparison circuit [12] and in various arithmetic circuits [13-14]. Modern computers processors are mostly implemented on 32 or 64 bits architecture [15-16]. Therefore, requirement of wide adders have become essential. Wide adder in Ripple Carry Adder (RCA) style results in excessive delay due to propagation of signals though the adder stages [17-18]. This excessive delay is not acceptable in modern VLSI circuits for which the concept of Parallel Prefix Adder (PPA) has evolved [19]. CLA [20], CSA [21], Carry Save Adder [22], Carry-Skip Adder [23], Manchester Carry Chain [24] are some of the well-known PPAs.

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CLA is considered as the most common adder topology among the PPAs for which extensive research has been conducted on this topic [25]. However, Majority of the research on CLA have been performed on logic and algorithm generation while only a handful amount of work in transistor level design have been conducted [26-30]. Therefore, it is quite necessary to develop a transistor level design of CLA which bring about overall performance of the entire CLA block.

In many design methodologies, 4-bit adder is considered to be a basic block to give rise to wide word length adders [31-32]. Therefore, optimization of 4-bit CLA will bring overall increment in performance of wide word length adder.

We have completed this research in 2 stages working with 3 types of adders. In the first stage, we have designed the conventional 4-bit carry look-ahead adder. Then, we modified the 4-bit CLA adder. We also designed a 4-bit ripple carry adder and made a comparison among conventional 4-bit CLA, modified 4-bit CLA and conventional 4-bit RCA. In the second stage, the proposed 4-bit CLA has been extended to 32-bit in CSA style to test performance in wide word length. The performance of the proposed 32-bit CSA based on 4-bit CLA has been compared with 32-bit conventional CLA based CSA and 32-bit RCA. The proposed design showed high-performance compared to the 32-bit RCA and conventional 32-bit CLA based CSA which proves its effectiveness in wide word length adder. We also made another comparison of 32-bit CSA adders which were designed in different ways.

The remaining portion of this article is organized in the following manner. Section II describes the design process of conventional CLA based CSA and RCA. Next, section III presents the proposed 32-bit CSA implementation. After that, simulation results have been presented in section IV. Finally, concluding statement is discussed in section V.

## II. DESIGN OF CONVENTIONAL ADDERS

In this section, the concepts of conventional 4-bit CLA, 32-bit CSA implementation process using 4-bit CLA and 32-bit RCA implementation process is described.

### A. Conventional CLA

A carry look-ahead is a type of adder used in digital logic circuits, that improves speed by reducing the amount of time to determine carry bits. It easily determines one or more carry bits before determining the sum. Thus, it helps to reduce the wait time to determine the higher value bits of an adder.

The conventional 4-bit CLA is implemented using static CMOS logic using carry propagate ($P_i$) and Carry Generate ($G_i$) terms (here $0 < i < 3$). If we consider $A_i$ and $B_i$ as the input bits which are required to be added, then the $G_i$ and $P_i$

  

functions can be written as [33-34]:

$$G_i = A_i\, B_i \quad (1)$$

$$P_i = A_i \oplus B_i \quad (2)$$

Based on equations (1) and (2), it is clear that $G_i$ represents AND function between $A_i$ and $B_i$ whereas $P_i$ represents XOR operation between $A_i$ and $B_i$.

The generic equation of 4-bit CLA in conventional style can be stated as [35]:

$$C_{i+1} = G_i + P_i C_i$$

Based on the generic equation, the specific CLA functions can be written as [36-37]:

$$C_1 = G_0 + P_0 C_0 \quad (3)$$

$$C_2 = G_1 + P_1 C_1 = G_1 + P_1 G_0 + P_1 P_0 C_0 \quad (4)$$

$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0 \quad (5)$$

$$C_4 = G_3 + P_3 C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0 \quad (6)$$

The schematics of the AND and XOR functions in conventional static CMOS logic are shown in Fig. 1. Sum in each stage is generated by cascading 2 XOR gates.

Based on the above equations, the schematic of the conventional 4-bit CLA carry terms are shown in Fig. 2 [38, 49].

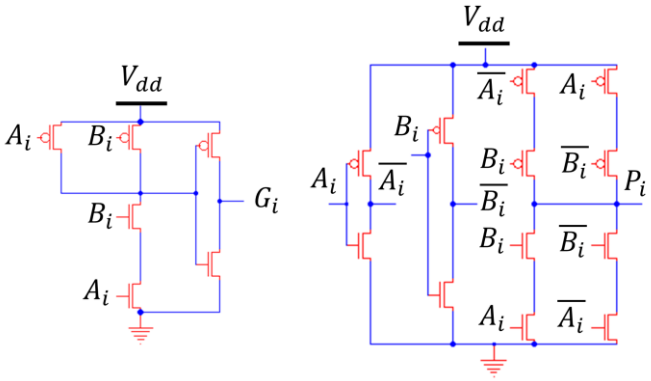


Fig. 1. Transistor level circuits for Conventional AND gate and XOR gate

### B. *Conventional CSA using 4-bit CLA*

A CSA is a type of logic adder that computes the (n+1)-bit sum of 2 n-bit adders. We have designed a 32-bit CSA using 4-bit CLA.

In CSA, the addition process in long chains is broken down into small groups. A n-bit CSA is mainly divided into (n/2)-bit section. In binary carry generation, the carry bit can have two distinct states: logic 0 and logic 1. Therefore, $C_{n/2}$ bit carry will also have those 2 distinct states:

$$C_{n/2} = 0 \text{ or } C_{n/2} = 1$$

Now, CSA utilizes two adders for upper word and an adder for lower word. Multiplexers are used to enable the necessary upper word based on the signal obtained from the lower word. Block diagram of 32-bit CSA is expressed using Fig. 3 [38]. Here, three individual 16-bit adder, one 2:1 Multiplexer for $C_{32}$ and 16-bit 2:1 Vector MUX (equivalent to 16 individual 2:1 Mux) are being used [49]. Design process of a 16-bit adder is presented in Fig. 4 where 4-bit CLA is being used as basic block.

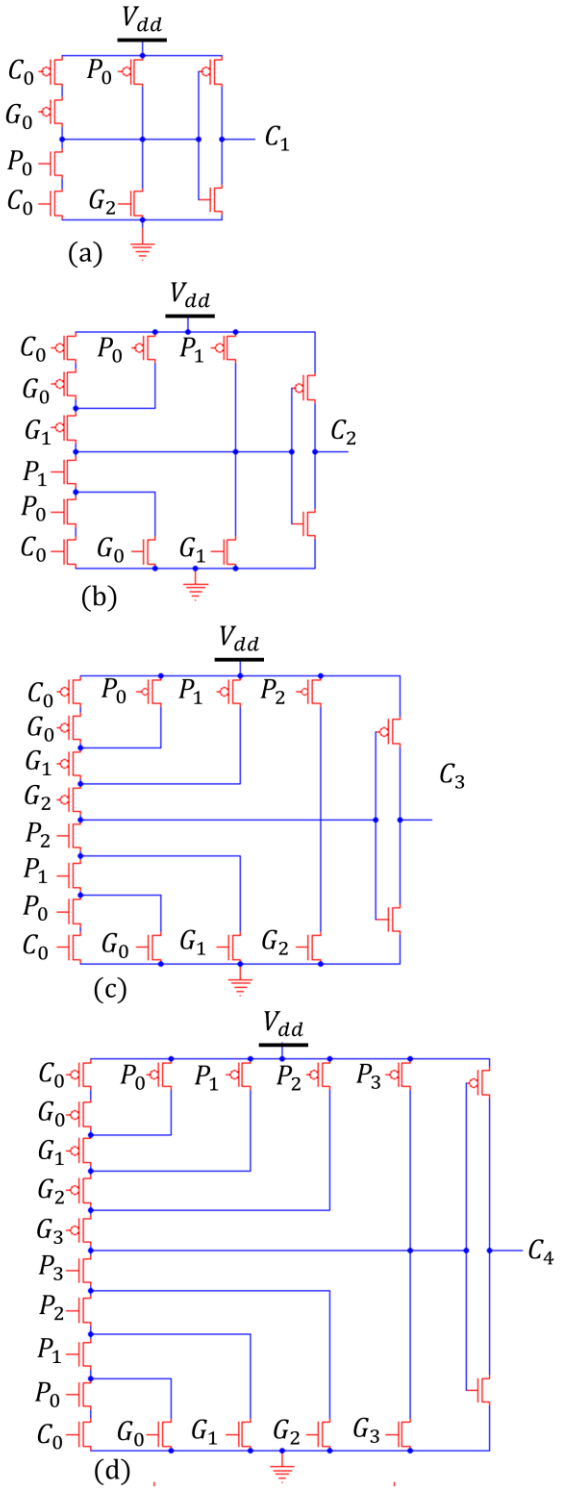


Fig. 2. 4-bit CLA Carry Architecture: (a) C1 circuit, (b) C2 Circuit, (c) C3 Circuit, (d) C4 Circuit.

### C. *Conventional RCA*

A RCA is a logic circuit whereas carry-in of next adder depends on the carry-out of previous adder. Here, sum and carry-out of any adder isn't determined until carry-in of that stage occurs. RCA adder has more delay comparing to other adders because of its long carry chains.

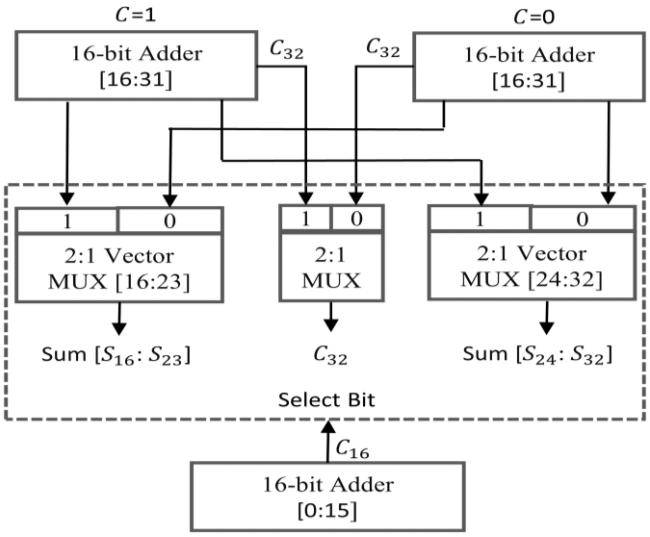


Fig. 3. Design of a 32-bit CSA

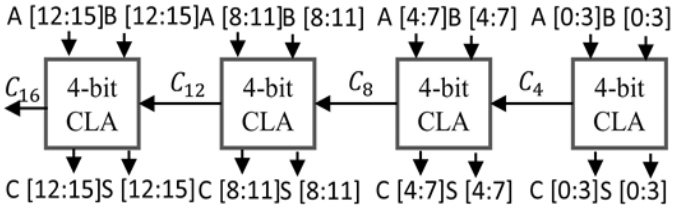


Fig. 4. Design of a 16-bit Adder Based on 4-bit CLAs.

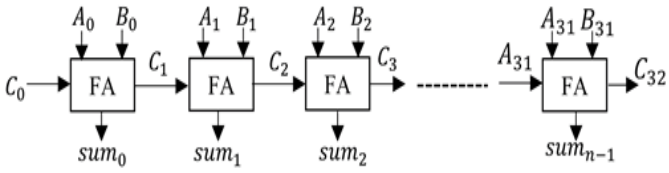


Fig. 5. Design of a 32-bit RCA.

Block diagram of a 32-bit RCA process is presented in Fig. 5 [39]. From Fig. 5, it can be understood that RCA possess thirty two full adder (FA) cells. There are various FA based on various logic techniques [40-44]. The adder in [44] would be used here to implement RCA due to its scalability. In RCA, computation of one adder stage needs to wait for its previous adder stage. For this reason, carry signals goes through all the adder stages for which delay increases in wide word length adders.

## III. Design of Proposed Adders

### A. Proposed CLA

The proposed 4-bit CLA uses the CLA carry terms presented in Fig. 2. However, the changes are made on XOR and AND gates for $P_i$ and $G_i$ functions. The proposed XOR and AND gates utilize hybrid logic approach unlike conventional static CMOS process. Truth table for $G_i$ and $P_i$ function is presented in Table I.

We have also presented Cadence design of our proposed 4-bit CLA in the Figure 08. The whole design was conducted in Cadence 90nm technology. Here, the connections of the design were completed through virtual wires.

#### 1) AND Gate Design

The proposed AND gate for Gi circuit implementation uses hybrid logic style. As per observation of Table 1, the following conditions apply for designing 2-input AND gate:

Condition 1: If $A_i = B_i = 0$, then $G_i = Gnd\ (logic\ 0)$
Condition 2: If $A_i = 0, B_i = 1$, then $G_i = A_i$
Condition 3: If $A_i = 1, B_i = 0$, then $G_i = B_i = Gnd$
Condition 4: If $A_i = B_i = 1$, then $G_i = A_i$

Based on the conditions 1-4, circuit diagram of the proposed 2-input AND circuit I presented in Fig. 6. As per Fig. 6, the following transistors are responsible for implementing the above-mentioned conditions 1-4.

Condition 1: implemented by $n_3$
Condition 2: implemented by $p_2$
Condition 3: implemented by $n_2$ and $n_3$
Condition 4: implemented by $p_2$

#### 2) XOR Gate Design

Unlike 2-input AND circuit, the proposed XOR circuit for Pi implementation uses hybrid logic style as well. As per observation of Table 1, the following conditions apply for designing 2-input XOR gate:

Condition 1: If $A_i = B_i = 0$, then $P_i = A_i = B_i$
Condition 2: If $A_i = 0, B_i = 1$, then $P_i = B_i$
Condition 3: If $A_i = 1, B_i = 0$, then $P_i = A_i$
Condition 4: If $A_i = B_i = 1$, then $P_i = \text{Gnd}$

Based on the above-mentioned conditions 1-4, circuit diagram of the proposed 2-input XOR circuit is presented in Fig. 7. As per Fig. 7, the following transistors are responsible for implementing the above-mentioned conditions 1-4.

Condition 1: implemented by $p_4$ and $p_5$
Condition 2: implemented by $p_5$
Condition 3: implemented by $p_4$
Condition 4: implemented by $n_4$ and $n_5$

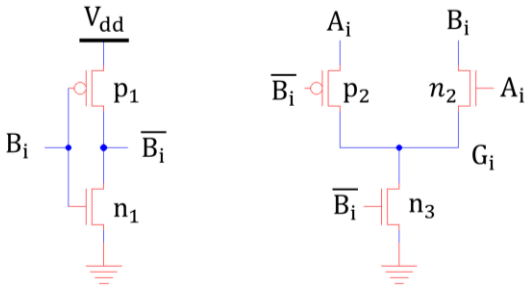


Fig. 6. Proposed AND gate circuit.

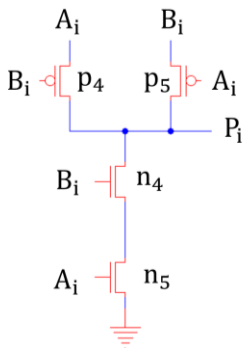


Fig. 7. Proposed XOR gate circuit.

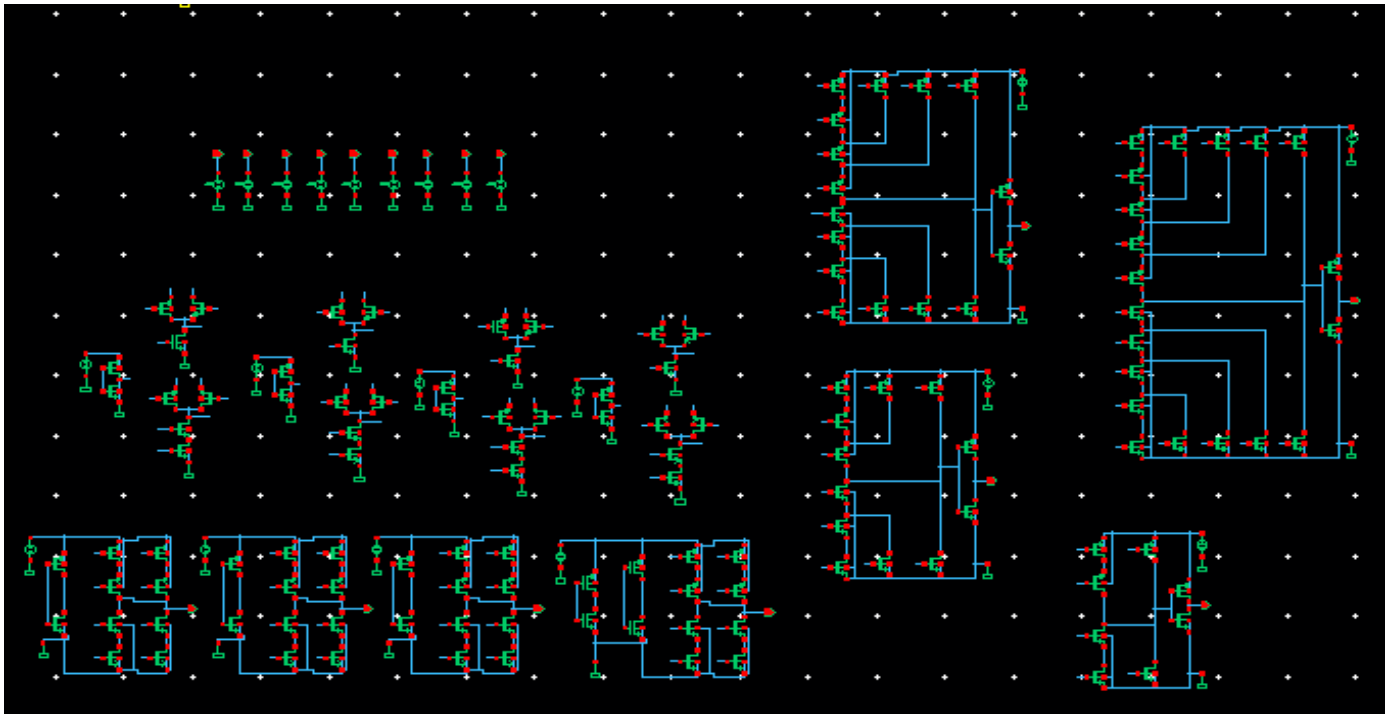

Fig. 8. Proposed design of 4-bit CLA

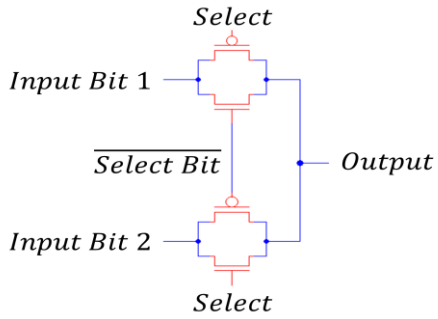


Fig. 9. TG 2:1 MUX used in proposed and conventional CSA.

TABLE I. TRUTH TABLE OF $G_i$ AND $P_i$

| Input | | Output | |
|---|---|---|---|
| $A_i$ | $B_i$ | $G_i$ | $P_i$ |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

### *B. Proposed 32-bit CSA implemented using Hybrid 4-bit CLA*

The block diagram for proposed 32-bit CSA is exactly similar to the conventional design in Fig. 3. The main difference lies in the 4-bit CLA part. In addition to the 4-bit CLA, the proposed CSA used Transmission Gate (TG) 2:1 Multiplexers (MUX) rather than using static CMOS logic. The TG 2:1 MUX is presented in Fig. 9.

## IV. SIMULATION RESULT AND COMPARISON

Performance verification of the proposed and conventional designs is evaluated using Cadence Virtuoso Tool [47]. Standard 90 nm technology node is utilized. Supply and signal voltages are 1 V. We have used channel width and length 120 nm and 100 nm respectively.

Detailed information on the performance of 4-bit adders and 32-bit adders are provided in the following sub-sections.

### *A. 4-bit adder performance comparison*

Performance parameters of 4-bit adder in proposed CLA, conventional CLA and RCA style is stated in Table II.

TABLE II. PERFORMANCE OF 4-BIT ADDER

| 4-bit Adder | Number of Transistors | Power (μW) | Delay (ns) | PDP (fj) |
|---|---|---|---|---|
| Conventional CLA | 170 | 55.4 | 0.16348 | 9.05 |
| RCA | 96 | 16.68 | 0.52159 | 8.70 |
| Proposed CLA | 130 | 38.82 | 0.13585 | 5.27 |

From the above table, we can say that the proposed design is considered to be the fastest adder topology while compared with conventional 4-bit CLA and RCA. Power consumption of RCA is lowest due to its less number of transistors [44-46]. The proposed 4-bit CLA also achieved predominant performance in Power Delay Product (PDP).

### *B. 32-bit adder performance comparison*

Performance parameters of 32-bit adder in proposed CSA, conventional CSA and RCA style is stated in Table 3. Graphical representation of the performance aspects has been depicted using Fig. 10. Unlike 4-bit adder, the proposed 32-bit CSA obtained superior speed while RCA obtained superior performance in power. PDP of the proposed 32-bit CSA is the lowest.

TABLE III. PERFORMANCE OF 32-BIT ADDER

| 32-bit Adder | Number of Transistors | Power (μW) | Delay (ns) | PDP (fj) |
|---|---|---|---|---|
| Conventional CSA | 1360 | 455.4 | 0.66792 | 304.1 |
| RCA | 768 | 138.7 | 4.1727 | 578.8 |
| Proposed CSA | 1140 | 322.6 | 0.55685 | 179.6 |

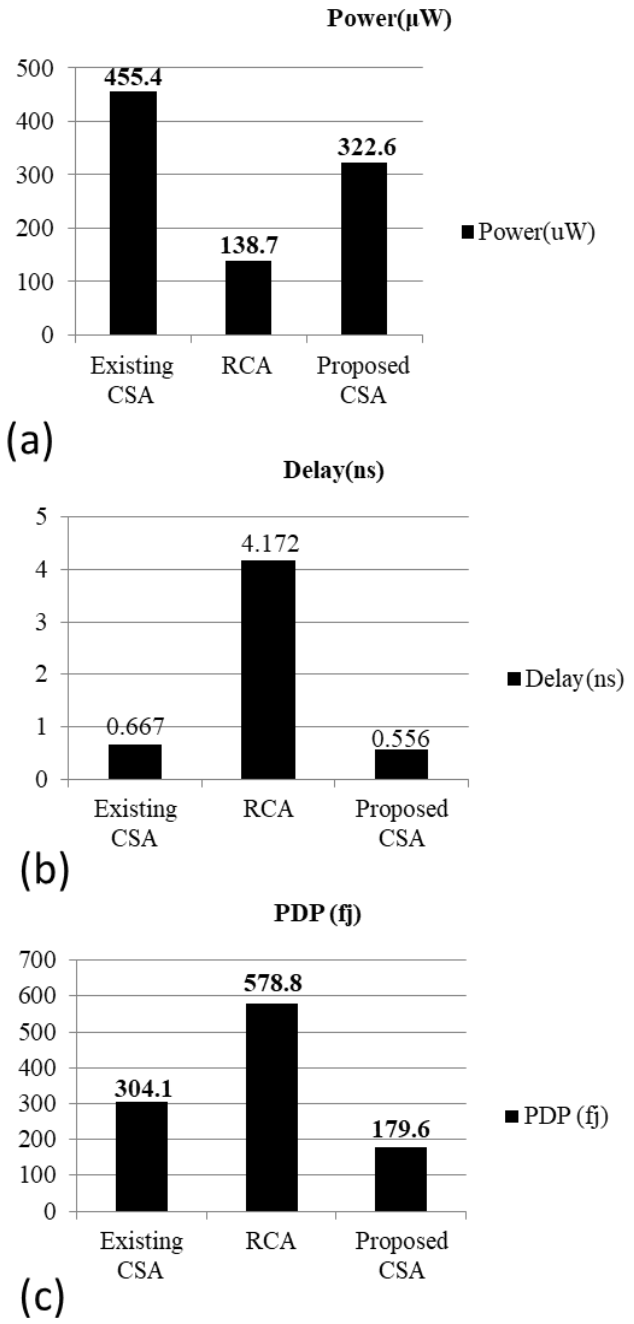


Fig. 10. 32-bit adder comparison (a)Power, (b)delay and(c) PDP

We have made another comparison of 32-bit CSA adder using different adder cell. We kept the same environment for the comparison. We have simulated on 90 nm technology using cadence tool and the supply voltage were 1V for all the references. This comparison is presented on Table 4. As presented on the table, [49], [51-52] & [56] presented high power consumption and [48], [50] and [54] had moderate value whereas [55] presented the lowest power consumption among all. In terms of delay, [48-50] and [54] showed a higher delay in comparison to other references. Here, [51] had the highest speed. Moving to the PDP, [53] and [55] had lower PDP. Comparing all the results, [55] had the lowest power but its delay was higher whereas [51] had the lowest delay but its power consumption was very high. On the other hand, our proposed design of 32-bit CSA adder had moderate delay as well as power consumption but it had the lowest PDP which is the key factor to evaluate overall performance. As a result, our proposed design again showed a tremendous performance.

TABLE IV. COMPARISON WITH OTHER REPORTED WORK OF 32-BIT CSA ADDERS OPERATING IN 1V SUPPLY VOLTAGE

| Ref. no | Power (µW) | Delay (ns) | PDP (fj) |
|---|---|---|---|
| [48] | 350.43 | 0.647 | 226.73 |
| [49] | 428.01 | 0.663 | 283.77 |
| [50] | 368.47 | 0.681 | 250.93 |
| [51] | 408.45 | 0.512 | 208.74 |
| [52] | 394.5 | 0.614 | 238.21 |
| [53] | 324.28 | 0.579 | 187.06 |
| [54] | 342.81 | 0.635 | 213.78 |
| [55] | 310.5 | 0.625 | 192.04 |
| [56] | 402.25 | 0.593 | 235.94 |
| **This work** | **322.6** | **0.566** | **179.63** |

## V. CONCLUSION

A hybrid method of 4-bit CLA adder is presented in this paper. The 4-bit CLA is then extended to 32-bits in CSA style. Performance of the proposed 4-bit CLA and 32-bit CSA is compared with the conventional RCA and CLA. Both the proposed 4-bit CLA and 32-bit CSA achieved predominant performance in speed while dissipating acceptable power. The PDP of the proposed designs (4-bit CLA and 32-bit CSA) were also the lowest as per the simulation conducted. We have also collected few data of different 32-bit CSA designs. Finally, we have presented the data and performed a comparison. Our proposed 32-bit CSA adder showed the best performance in terms of Power, delay and Power delay product. Hence, the PPAs in this work can be highly useful in high-performance ALU design in modern systems.

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