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Temperature Characteristics of Nano-Dimensional FinFET with P Type GaP Semiconductor Channel Based on I_{ON}/I_{OFF} and Subthreshold Swing (SS)

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***Abstract*— This study explores the effect of operating temperature on the performance of GaP-FinFET structures. The Multi-Gate Field Effect Transistors (MuGFET) simulation tool was employed to analyze the electrical characteristics of FinFETs across a temperature range of 0 °C to 125 °C. A P-channel GaP-FinFET with constant channel fin parameters was simulated to investigate its current-voltage behavior under varying thermal conditions. The findings reveal a significant variation in current (ΔI) within the gate voltage range of -0.7 V to -1 V, demonstrating the potential of P-channel GaP-FinFETs as nanoscale temperature sensors. The highest ΔI and temperature sensitivity were observed at Vg = -1 V. However, increasing the operating temperature led to degradation in subthreshold swing (SS) and the I_{ON}/I_{OFF} ratio, indicating a trade-off between sensitivity and device performance.**

***Index Terms*—FinFET, MOSFET, temperature, nano, transistor.**

I. Introduction

As the typical silicon metal-oxide-semiconductor field-effect transistor (MOSFET) gets closer to its scaling down limitations, many novel transistor topologies have been studied in detail. Among these, the semiconductor and academic communities have shown a great deal of interest in the Fin Field Effect Transistor (FinFET). In order to handle the fault of the minimizing MOSFET structure towards nanoscale region, researchers are currently exploring new transistor structures with nano-dimensions, such as FinFETs [1-3]. The Fin field-effect transistor (FinFET) structure is one of the most significant structures.

With FinFETs providing sustainable performance at lower technology nodes, MOSFETs have been successfully replaced in key semiconductor industries such as Intel, Samsung, TSMC, etc. When compared to traditional MOS devices, this device's primary draw is its superior gate controllability via numerous fins over the active channel. Due to the reliance of carrier transport on temperature, it is one of the critical parameters whose influence on device performance can never be disregarded.[4]

FinFETs are an ideal substitute for Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) in standard configurations [5]. They are utilized in electronic circuits with nanoscale dimensions because of their exceptionally low threshold current (I_{OFF}), lower sub-threshold swing (SS) under limit value (60 mV/decade), reduction of short channel effects, and excessively low power consumption. [6–10].

Circuit performance changes as a function of operating temperature because the electrical properties of semiconductors in FinFET, such as band gap , carrier density, mobility, velocity saturation, threshold voltage (V_T), and leakage current, are highly dependent on temperature. Consequently, it's critical to investigate any potential high-temperature degradation that can result in a hot temperature corner where performance is compromised. The temperature sensitivity of the FinFET device is useful to understand and model in order to facilitate the design of circuits using this technology. [11]

The FinFET structure is depicted in Fig. 1, and this research work discusses the temperature characteristics of this nanostructure and the possibilities of employing it as a nano-sensor for temperature.

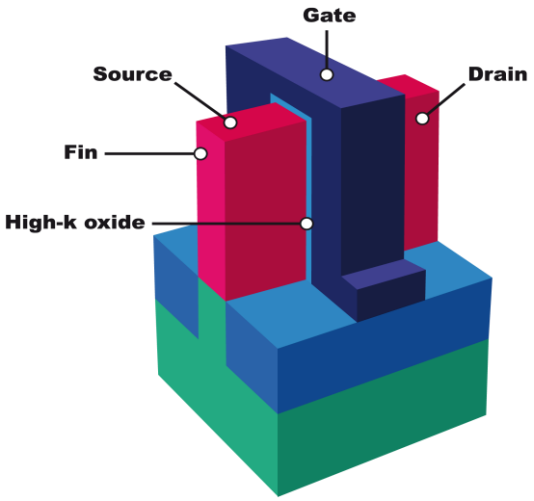

Fig. 1 FinFET structure.

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II. Methodology

The use of simulation tools has become increasingly critical for analyzing electronic devices, as they provide insights into the fundamental physics governing the architectures of emerging technologies. These tools are also instrumental in evaluating the scalability of nano-dimensional devices, as well as assessing their advantages, limitations, and potential cost-saving measures. .[12]

In this study, the I-V characteristics of a FinFET structure with a P-type Gallium Phosphide (GaP) semiconductor channel (GaP-FinFET) were simulated. Key parameters included a channel length of 10 nm, a doping concentration of 10^{16} cm^{-3}, source and drain lengths of 5 nm, and an SiO_2_22 oxide thickness of 1 nm. The width of the fin-shaped gate was set to 3 nm. Simulations were conducted across various operating temperatures, specifically at 10 °C, 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C.

This work employs the MuGFET simulation tool to model and analyze the performance of the P-channel GaP-FinFET transistor [13]. The study focuses on generating output characteristic curves under varying conditions and configurations. Furthermore, the influence of operating temperature on the device was evaluated through the simulated I-V characteristics. MuGFET, a simulation tool designed for modeling nano-dimensional FET structures, was developed by Purdue University and is widely used for this purpose.

Bell Laboratories produced both PADRE and PROPHET, the two simulation solutions available for MuGFET. Whereas PADRE is a device-oriented simulator for 2D or 3D devices with changing geometry, PROPHET is a partial differential equation profiler for one, two, or three dimensions [13]. When the program properly describes the mechanics of FETs, it can produce distinctive FET curves that are useful for engineers. When computing channel characteristics, MuGFET can be utilized to mimic the motion of transport items and produce self-consistent solutions to the Poisson and drift equations [13].

The output characteristics (Id-Vg) of P-channel GaP-FinFET has been simulated using MuGFET tool [13], and Fig. 2 represent the symbol for P-channel GaP-FinFET where all currents and voltages must be in negative form.

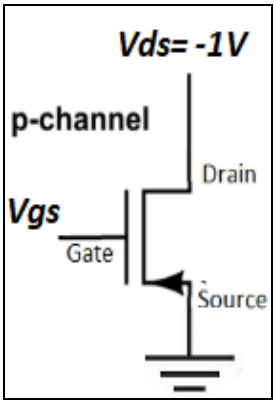

Fig. 2 P-channel FinFET with Vds= -1 V.

III. Results

As an example, the transfer characteristics of the P-channel GaP-FinFET at 25°C working temperature has been clarified in Fig. 3 at V_{ds} varied from 0 to -1V step down -0.1V. Fig. 4 presents the output characteristics curves of the P-channel GaP-FinFET at gate voltage from 0 to -1 step -0.1V at working temperatures of 25°C. To simulate the Id-Vg characteristics of each FinFET condition separately, the MuGFET tool [13] was utilized.

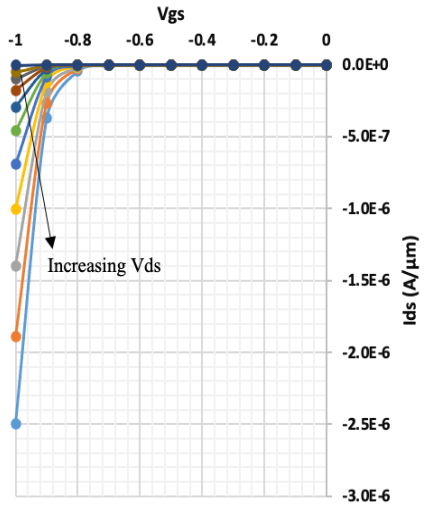

Fig. 3 N- and P-channel MOSFET connected in diode mode (Vd=Vg)

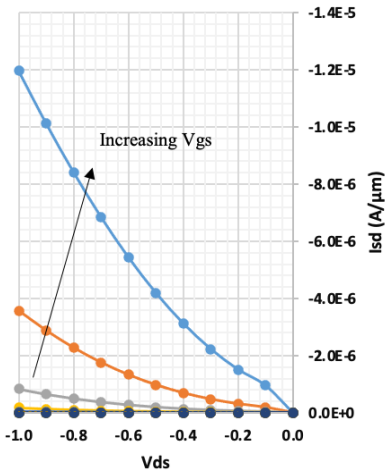

Fig. 4 Current-voltage characteristics at working temperatures of 125 °C.

However, Fig. 5 shows the same features under the same circumstances, but at 125 °C for the operating temperature. These characteristics make it evident that current increases as the working temperature rises. This is because the semiconductor's band gap narrowing effect and the increase in intrinsic carrier concentration with temperature permit the doping concentration to affect the I-V characteristic and threshold voltage of the MOS structure when it operates at higher temperatures. [14]

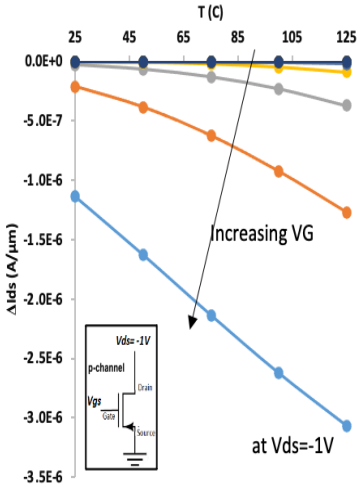

Fig. 5 ΔI-T characteristics at Vds=1V and gate voltages 0 to -1 V.

The results presented in Fig. 6 depict the variation in current change (ΔI_{ds}) for a p-channel GaP-FinFET device at a fixed drain-source voltage (V_{ds}=−1 V), over a gate voltage (V_{gs}) range of 0 V to −1.0 V. The measurements were carried out at operating temperatures ranging from 0°C to 125° C in 25° C Cincrements. The analysis highlights that (ΔI_{ds}) remains negligible for gate voltages above −0.6 V indicating minimal conduction or near cutoff behavior in this range. However, a significant increase in (ΔI_{ds}) is observed when the gate voltage transitions from -0.6 V to −1.0 V, suggesting strong gate control and active channel conduction within this voltage range.

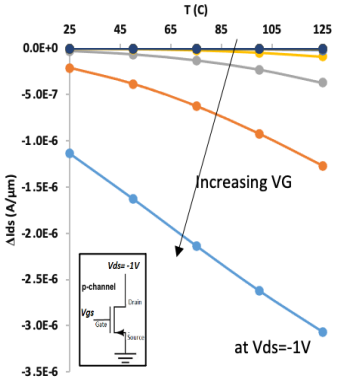

Fig. 6 ΔI-T characteristics at Vds=1V and gate voltages 0 to -1 V.

Notably, the results demonstrate a clear dependency on temperature. As the operating temperature increases, the onset of (ΔI_{ds}) occurs slightly earlier (closer to -0.6 V), and the rate of increase in current is more pronounced at higher temperatures. This trend can be attributed to thermal effects that enhance carrier mobility or reduce the effective barrier for hole conduction in the p-channel. At higher temperatures, the device exhibits improved conduction, as evident from the steeper rise in current at lower gate voltages. These findings suggest that the GaP-FinFET operates efficiently in the gate voltage range of -0.6 V to −1.0 V, with temperature playing a critical role in modulating the device's current response.

The results indicate that the p-channel GaP-FinFET is well-suited for applications requiring precise gate control in this voltage range. Additionally, the observed thermal behavior underscores the importance of temperature considerations in optimizing device performance for practical applications.

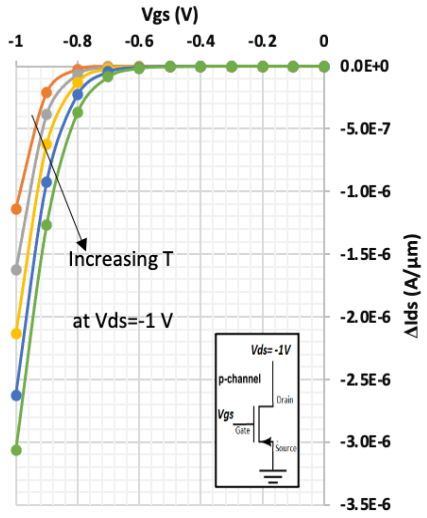

Fig. 7 Current-voltage characteristics at Vds=-1V and working temperature from 0 to 125 °C.

Fig. 7 represent the change in current (ΔI) of P-channel GaP-FinFET at V_{ds}=-1 V with working temperatures range from 25 to 125°C at gate voltage = 0 to -1 V step -0.1 V. The ΔI increase with increasing gate voltage (at V_{ds}= -1V) with all the range of temperature but the higher ΔI happens at higher gate voltages (Vg ≥|-0.7| V). As can be seen in this figure, for P-channel GaP-FinFETs, the temperature sensitivities are represented by ΔI, which is too low outside of this working voltage range. The higher ΔI occurs at higher temperature steps for the working voltage range (-0.7 to -1 V).

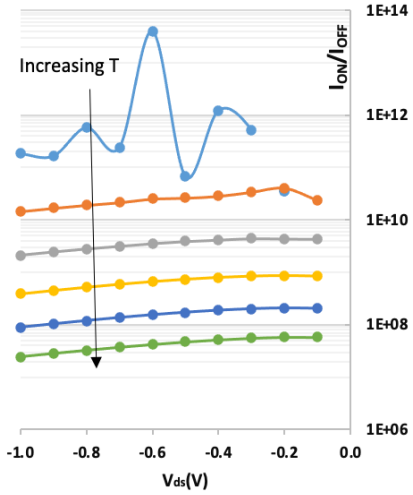

Fig. 8 (I_{ON}/I_{OFF}) with working voltage at working temperatures of 0, 25, 50, 75, and 100°C for P-channel FinFET.

Figure 8 illustrates the current ratio (I_{ON}/I_{OFF}) between ON (at Vgs=-1V) and OFF (at Vgs=0V) at a working voltage (V_{ds}) range of 0 to 1 V when the working temperature increases by 25°C step up (ΔT=25°C), that is, at temperatures between 0, 25, 50, 75, and 100°C. The ON to OFF current ratio (I_{ON}/I_{OFF}) at various working voltages (0V to -1V step down -0.1 V) and a temperature range of 25 to 125°C V is shown in Fig. 9.

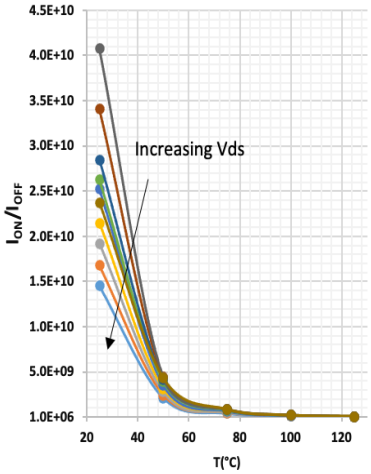

Fig. 9 (I_{ON}/I_{OFF}) with working temperature at working voltages -0.1 to -1V step -0.1 for P-channel FinFET.

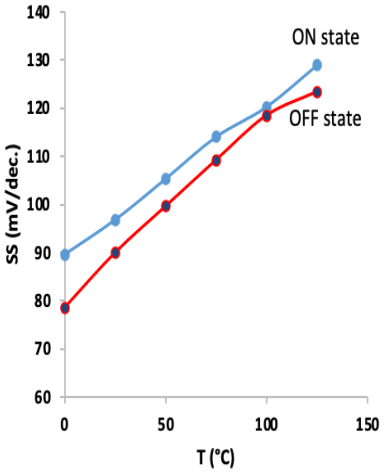

Fig. 10 Sub-threshold swing (SS) versus temperature characteristics.

Figure 10 depicts the temperature-dependent variability in Subthreshold Swing (SS). SS is defined as the slope of the Ids vs Vgs graph, where Ids is scaled logarithmically. SS grows linearly as the temperature rises. The optimal SS is the lower one, with an optimal value of 60 mV/dec. The lowest SS value was discovered at 0°C for both the ON and OFF states, which also happened to be the best values. FinFETs can be employed in electronic circuits with lower temperature requirements to achieve lower SS and a higher ION/IOFF ratio due to the results for I_{ON}/I_{OFF} and SS with temperature characteristics.

IV. Conclusion

This research provides a comprehensive analysis of the effects of operating temperature on the electrical behavior of P-channel GaP-FinFETs. By utilizing the MuGFET simulation tool, the temperature-dependent characteristics of these nanoscale devices were evaluated over a range of 0 °C to 125 °C. The findings reveal that the gate voltages range of -0.7 V to -1 V is particularly significant, as the device exhibited maximum current variation (ΔI) and temperature sensitivity at higher operating temperatures. Notably, sensitivity showed a linear decline as temperature decreased, confirming the strong thermal dependency of the device's performance. Furthermore, the maximum ΔI and temperature sensitivity were observed at Vg = -1 V, highlighting its suitability for nanoscale sensing applications.

However, the performance metrics such as the subthreshold swing (SS) and the I_{ON}/I_{OFF} ratio deteriorated with increasing temperature. At 0 °C, the device demonstrated its best SS values, measuring 78.6 mV/decade in the OFF state and 89.7 mV/decade in the ON state. These findings underscore a trade-off between temperature sensitivity and the overall performance of P-channel GaP-FinFETs at elevated temperatures. This work provides valuable insights for optimizing GaP-FinFETs for applications requiring high sensitivity and stability across varying temperature ranges.

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